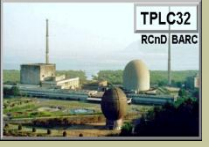

Trombay Programmable Logic Controller TPLC-32

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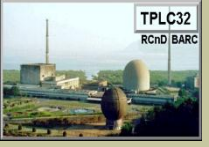
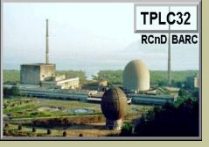


Overview

- Safety and Safety Related Computer Based Systems (CBS) in NPP
- Development and Regulatory Efforts for System Qualification
- Why Qualified programmable Configurable platforms
- TPLC-32 Platform , Development process and Salient features
- System Configuration and FBD Editor
- Build ,Offline Simulation and Run time debugging
- Systems Developed using TPLC-32
- Enhancements in New Version

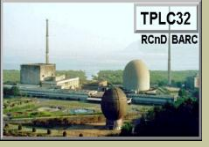


Requirements of CBS in NPP

- In Addition to functional, performance and interface requirements, Safety and safety related CBS in Nuclear Power Plant have to meet stringent regulatory requirements like enhanced reliability, safety, security, fault tolerance, diagnostics and self-supervision.

- Computer based systems have capability to implement complex functions, provide improved monitoring of plant variables, improved testing, calibration, self checking and fault diagnostic facilities. However, these features add to complexity of software.

- Unlike hardware faults, the software faults always result from errors in requirements, design or implementation and processes like wear-out, degradation and environment effects do not apply to software.



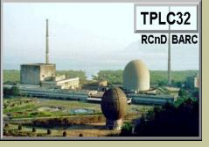
Safety and Reliability

- Computer Based Systems are not amenable to quantitative assessment of reliability due to software component of these systems. Therefore Assessment of software in the computer-based systems has to be based on evidence that the software is correct with respect to specifications, safe and completely implements the requirements.

- These systems must be demonstrated to be safe and reliable with appropriate degree of confidence.

- The software in these systems must be demonstrated to have high level of integrity. Integrity is defined as quality of completeness, dependability and freedom from defects.

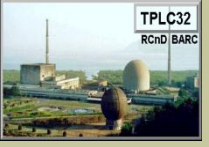
- This is confirmed through regulatory review process consisting of rigorous Verification and validation by Independent team of expert followed by further Audit by Regulatory Body.



Design and Regulatory Review Efforts

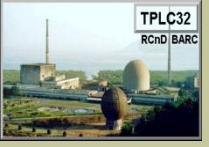
- Though, the designs of digital C&I systems in Indian NPPS have evolved in past three decades, most of these systems are still custom built systems.
- From plant to plant, due to requirement changes partial or major software changes are required. In some cases, complete software is to be redeveloped.
- Thus enormous development, IV&V and regulatory audit efforts are required for qualifying Custom built systems for use in NPP
- This influences over all plant commissioning schedule
- Further for Custom Build Systems, implementation of Requirement Change Request during plant operation is complex and time consuming process

Solution: System Development Based on Qualified Platform



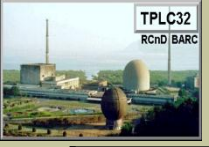
Benefits of Qualified Platform

- No need to develop low level complex system software
- System configuration & application development carried out by process / C&I engineer s trained on the platform.
- Reduced application development time with help of graphical programming framework like Function block diagram.
- Since platform is qualified, IV&V is to be carried out only for the Application.
- Verification of Programs in application oriented language like function block diagrams is easy and can be carried out by domain experts who need not be software specialist.
- Time required to develop and qualify the system is drastically reduced.
- Inbuilt testing function in the platform facilitates in detailed testing of the application.
- Ease in implementation of requirement change during system development and after deployment in plant.



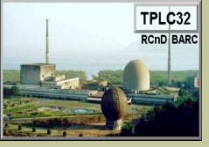
CBD-Custom build Design Against QPD: Qualified Platform Based Design

Features	CBD	QPD
Software design & Development	Enormous software development and needs specialized experts.	Application development by C&I and process engineers. Quick Development with graphical Function block based programming tools.
Verification & Validation	Enormous efforts and needs specialized experts	As platform is already qualified, V&V is to be carried out only for application. Application V&V can be done by domain expert with knowledge of Application languages
Cycle time estimation	Early time estimation is difficult & is based on assumptions. Any mistake have adverse impact at later stage on system architecture.	Inbuilt time estimation features gives conservative time estimates in advance and accordingly system architecture can be designed.



Features	CBD	QPD
Determinism	Lot of tests and analysis need to be carried out to ensure determinism	In built in the design, supported by time estimation features.
Implementation of RCR	Usually large as Basic design is to be modified and large V&V efforts.	Quick . Can be implemented at Site . Platform tools facilitates through testing of changes before deployment.
Designer Dependence	For even a very small change in application designer is required.	No dependence on designer. can be done by Design office/utility.
Regulatory Efforts	Large during initial design as well as for RCR	Dependence on Software experts is reduced.

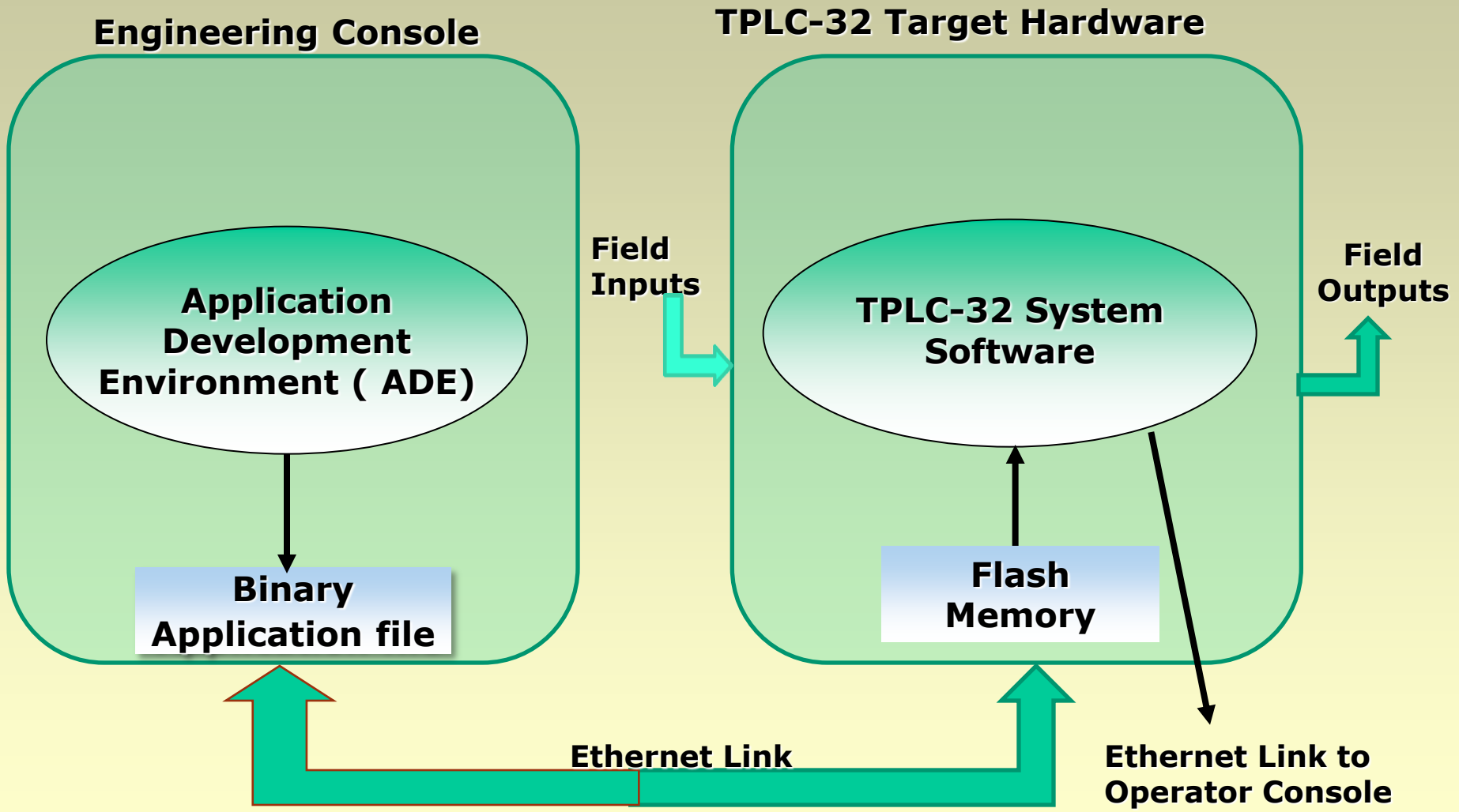
A Qualified platform **"Trombay Programmable Logic Controller TPLC-32"** Developed By BARC offers all these benefits

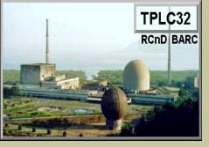


TPLC-32 Platform

- It Consists of a PC Based Engineering Console (EC) which can be linked to TPLC-32 hardware over Ethernet interface.
- The TPLC-32 hardware is designed around in house developed single board computer based on 32 bit processor and intelligent I/O boards and Ethernet boards.
- Application Development Environment (ADE) software on the EC provides the framework to configure, test, build and down load applications on TPLC-32 hardware.
- The TPLC-32 embedded system software executes the downloaded application.
- The TPLC-32 embedded system software executes under control of in house developed small foot print Real Time Kernel ESOS

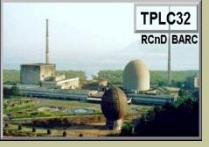
TPLC-32 Platform Architecture





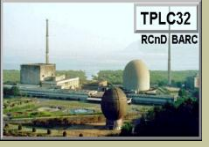
TPLC-32 Platform Development Process

- Systematically Controlled well documented development process based on AERB SG D25 and IEC 60880-2.
- 37 Design Documents as per the design process.
- Application software development with Function blocks based on IEC 61131-3 Standard.
- Platform Verification and Validation carried out by an Independent team
- Complete in-house design with associated documentation assures long term support, scalability and solutions against continuous changes in technology.



TPLC-32 Platform Salient Features

- Cycle Time Estimation
- Deterministic Performance
- Robust Diagnostics
- Fail safe and Simple design
- Offline testing
- Fault Tolerant design
- Hot Pluggable I/O modules
- Modular and Scalable
- User-friendly GUI



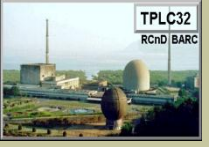
TPLC-32 Platform Salient Features

Cycle Time Estimation

- For a successfully build project, ADE estimates cycle time of the application to be executed on the TPLC-32 target hardware.
- The system developer gets the time estimates on ADE well before buying the hardware.
- In case the estimated time is not meeting the timing requirements of application:: The developer can optimize the developed application if possible or the deployment can be done in distributed manner on multiple nodes.
- The time estimation functionality very useful in early development to plan the hardware architecture and resources to meet application timing requirements.

Deterministic Performance

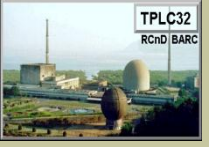
- TPLC-32 system Software sequentially executes all processing , control and safety functions at fixed cycle time under all load conditions without any jitter.
- Ensures Deterministic execution of diagnostics on hardware and Software.



TPLC-32 Platform Salient Features

Robust Diagnostics

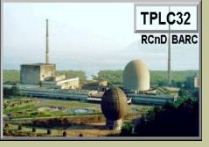
- Diagnostics check on all I/O hardware modules at 1 second periodicity. Board is declared as faulty if fault persists for two consecutive cycles.
- On failure detection, time stamped Diagnostics message to OC detailing failure in the board and Failure indication of fascia panel of the failed module.
- Check on integrity of System software, application software & alterable parameters at periodicity of 30 seconds.
- Check on Software program flow ensuring correct execution of all control and safety function every cycle in required sequence.
- Software self supervision for timely execution of control and safety function.
- Gross health status on alphanumeric display on CPU board.
- Hot replacement of Faulty Modules detected by diagnostics.



TPLC-32 Platform Salient Features

Failsafe Features

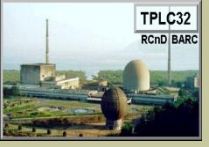
- On detection of input module failure, for all further processing , it uses predefined failsafe values for input signals assigned to the failed module.
- On Output board failure, it uses the predefined safe output values.
- On failure detection, the system stops accessing failed digital output modules and on non access these modules generate de-energized output.
- In case of software integrity check failure, the system generates failsafe outputs.
- Watchdog detects Gross software failure and generates predefined failsafe outputs.
- Health status every IO module is available for use in application program. Special function block facilitates generation of failsafe output.



TPLC-32 Platform Salient Features

Simple Design

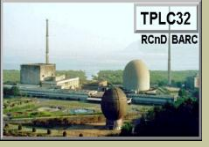
- Highly modular software design based on TOP-DOWN design approach with high cohesion and low coupling.
- Use of in-house developed small footprint pre-emptive multitasking kernel having predefined static task priority structure.
- No run time memory allocation .
- Usage of interrupts is restricted, only for essential activities like time keeping in kernel and handling of bus errors.
- Hardware redundancy at System level
- Simple, User friendly, Tree control based GUI for System configuration and Application development
- Fault tolerant implementation possible during system configuration
- Ease of maintenance due to automated on line fault detection and annunciation.



TPLC-32 Platform Salient Features

Cyber Safe

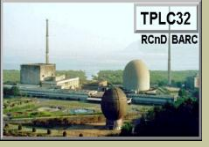
- The TPLC-32 Software has been fully reviewed through independent V&V process and does not contain any malicious code.
- The System and Application software is stored in Flash memory on processor board and checked for integrity at part of diagnostics.
- For changing the software, physical access is required to the cabinets which are located in secured area in the plant.
- Further the flash memory is programmed through a special in-house developed robust proprietary software which also have pass key checks.
- The TPLC-32 based systems provides only one way communication via intelligent Ethernet boards to Operator Console.
- The TPLC-32 system software has no software component to pickup data packets from Ethernet board giving total security against any attack.



TPLC-32 Platform Salient Features

Modular and Scalable Hardware

- A Single Node of TPLC can be configured for up to three 19 Inch Bins accommodating up to 43 I/O modules.
- Any Combination of I/O modules as per the application need can be configured.



TPLC-32 Platform Hardware

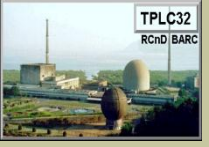
VME Single Board Computer: PowerPC 7447A @ 600 MHz

VME Ethernet communication Module : On board 80186 processor with Real time TCP/IP Stack, Dual media interface with Support for fiber media

Protocol Translator Module: Bridge VME with I/O bus

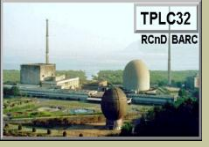
Intelligent I/O Modules: Board Controller implementation in FPGA using VHDL, Hot pluggable Design with On board self testing features

- Digital Output board: 32 Outputs
- Digital Input board: 32 ((Voltage/contact) Inputs
- Analog Input -Output Board: 32 inputs, 8 Outputs, ADC/DAC resolution 16 bits.
- Relay Output board: 16 outputs with User Selectable NO/NC contact



TPLC-32 I/O Capacity

- CPU Bin with 5 Slot VME backplane Accommodates CPU Board, two network board and protocol translator board interfacing VMR BUS with proprietary I/O bus.
- One CPU Bin and two Extensions of I/O Bin
- Geographical addressing of I/O Boards
- 15 slot Backplane I/O Backplane
- 9 slot Backplane I/O Backplane
- Any combination of 43 I/O boards supported with 9 slot I/O backplane in CPU bin and 15 slot I/O backplane in Extension bin
- One node can handle maximum up to 1248 input /outputs.



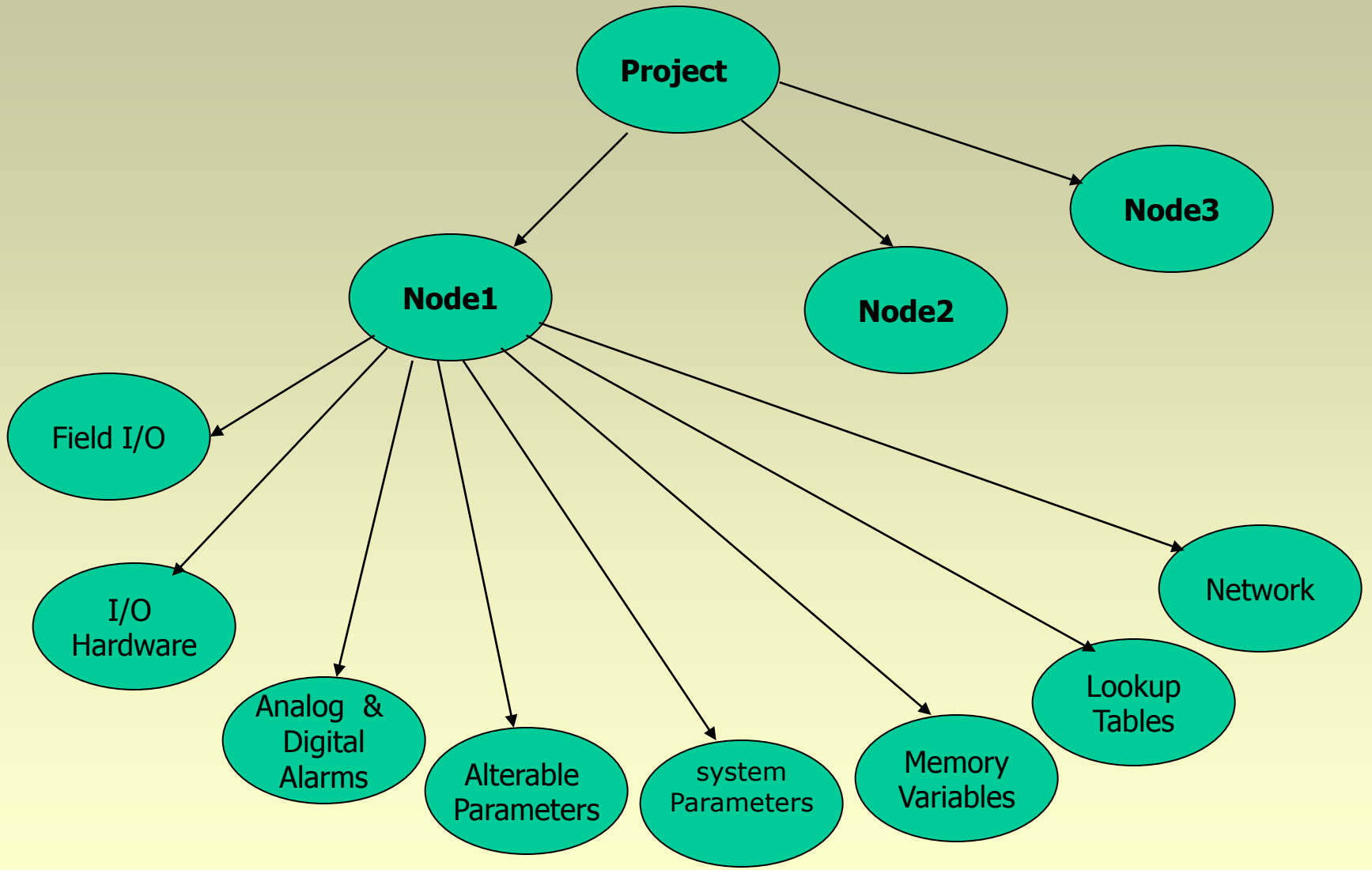
TPLC-32 Application Development Environment

- Features for complete system configuration with help of tree control based GUI.
- Application development using graphical programming language based on Function blocks.

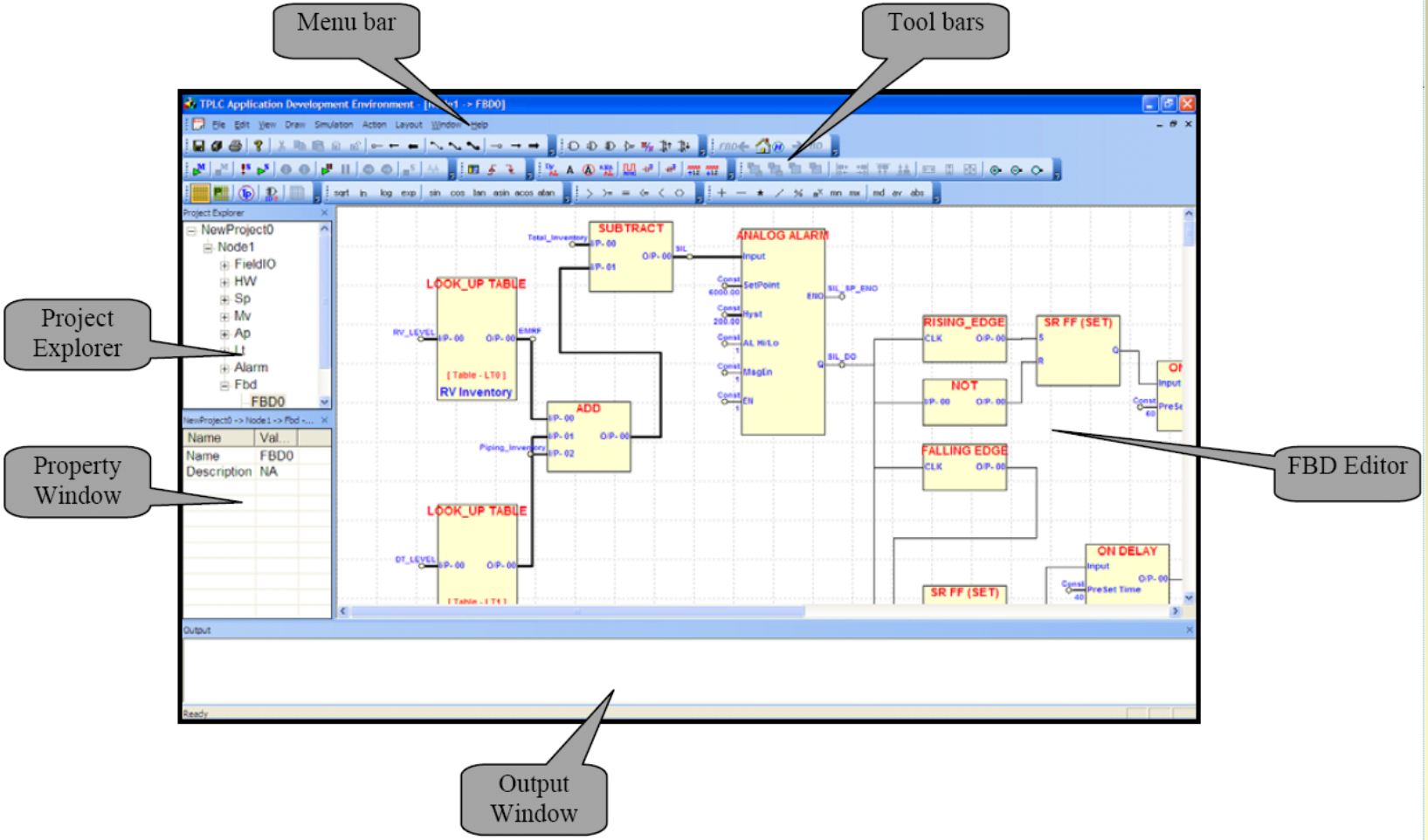
System configuration attributes

- Field inputs and outputs (Analog and digital)
- I/O Hardware Modules
- Assignment of Field I/O to channels on I/O hardware
- Analog and digital Alarm tags
- Alarm Annunciation groups and Lookup tables
- Memory variables
- Alterable Parameters / System Parameters
- Network Configuration

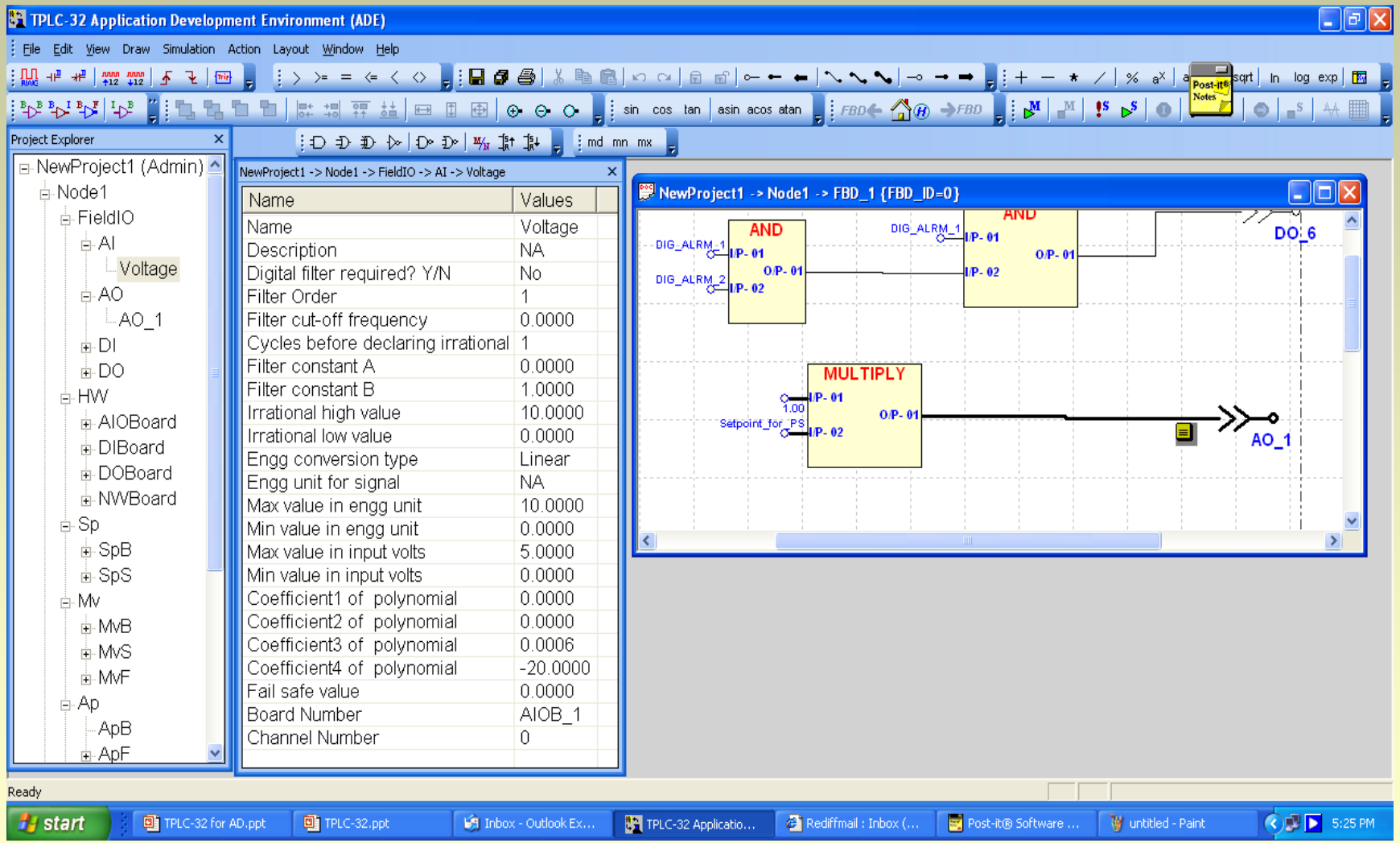
Configurable Attributes in system Configuration



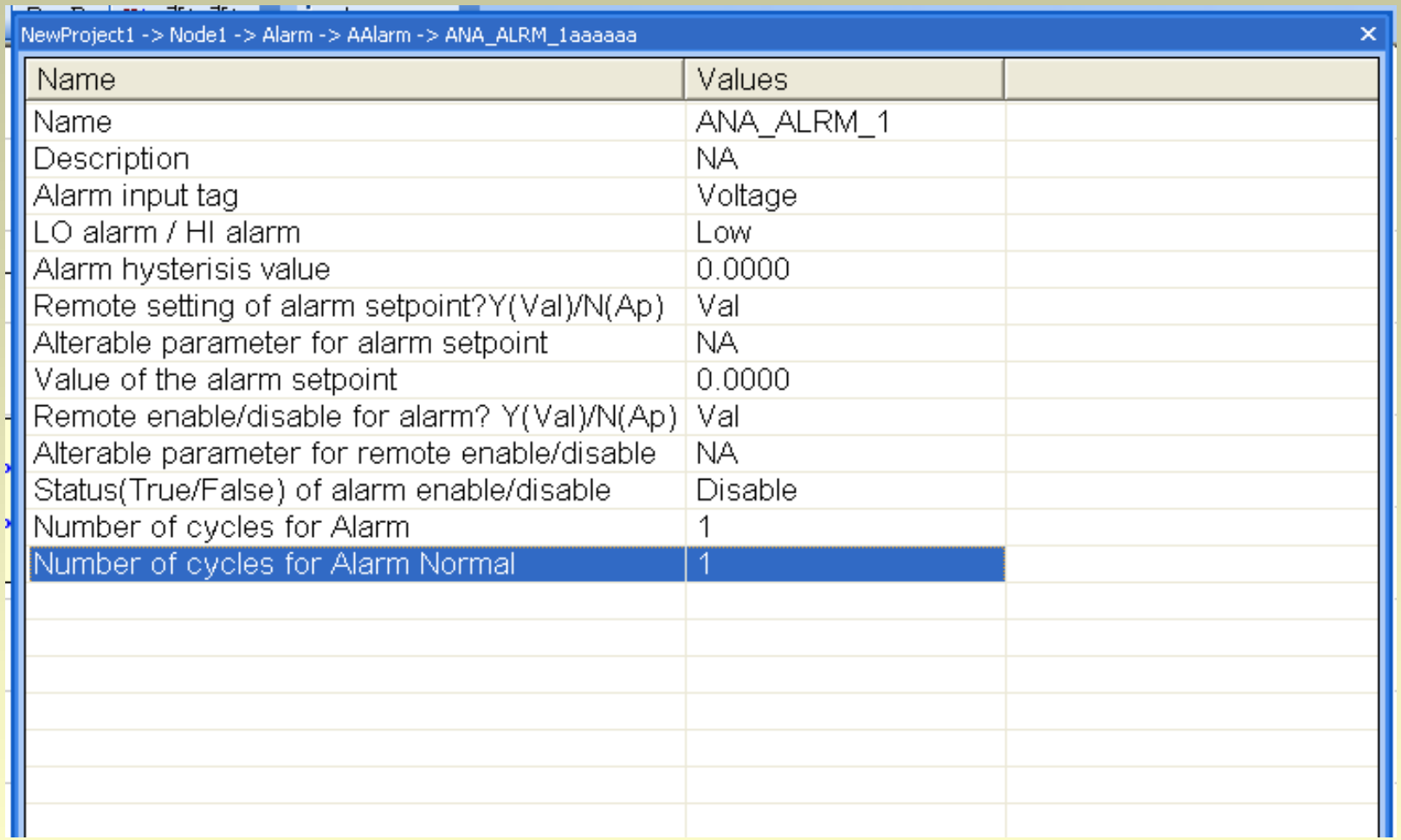
ADE Snap Shot



Configurable attributes of Analog Input

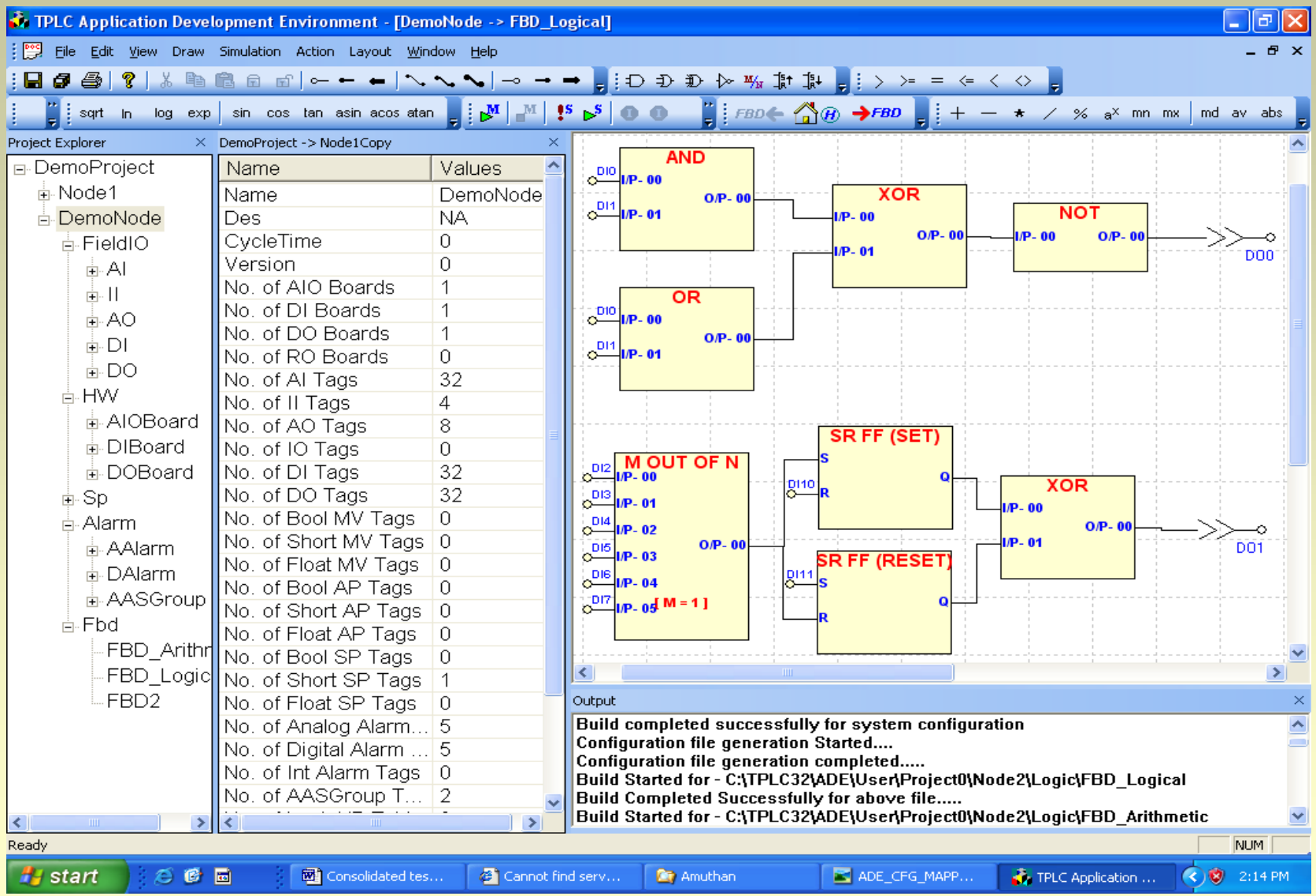


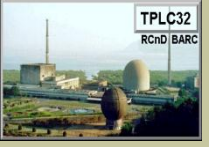
Configurable attributes of Alarm Tag



Name	Values
Name	ANA_ALRM_1
Description	NA
Alarm input tag	Voltage
LO alarm / HI alarm	Low
Alarm hysterisis value	0.0000
Remote setting of alarm setpoint?Y(Val)/N(Ap)	Val
Alterable parameter for alarm setpoint	NA
Value of the alarm setpoint	0.0000
Remote enable/disable for alarm? Y(Val)/N(Ap)	Val
Alterable parameter for remote enable/disable	NA
Status(True/False) of alarm enable/disable	Disable
Number of cycles for Alarm	1
Number of cycles for Alarm Normal	1

Screen Shot of Project Summary



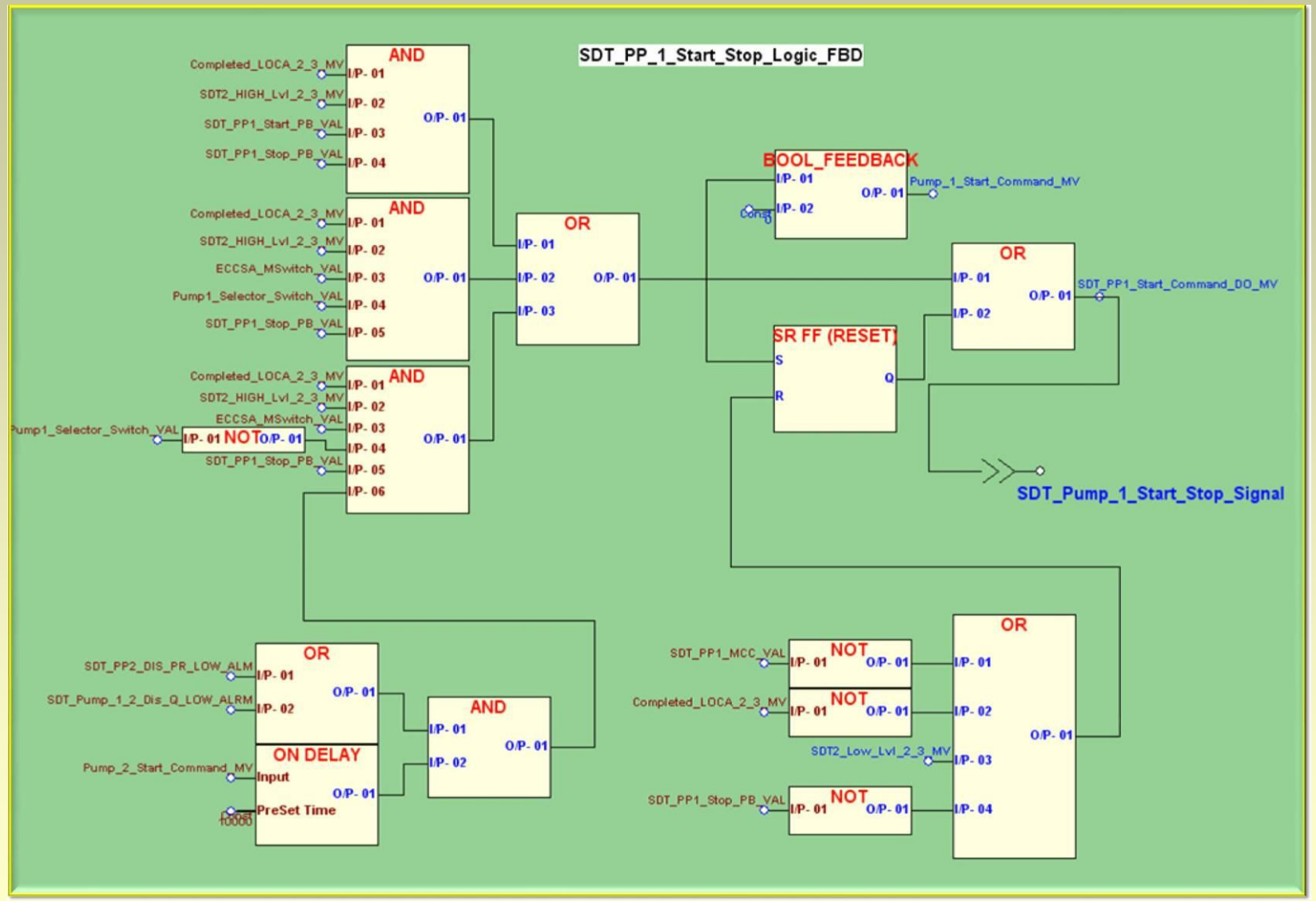


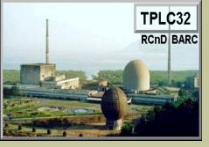
Function Block Diagram (FBD) Editor

FBD editor provides graphical programming environment to implement the application programming requirements, process logics in the form of function block diagrams.

- Provide features to select a function block from tool bar/menu and place it in to the FBD drawing area.
- Facilitates move/resize/copy of a selected function block.
- Allows assignment of configured analog inputs, digital inputs, alarm tag status, memory variables, alterable parameters, system parameters, hardware board status to the inputs of the function block.
- Facilitates to store the output of a function block in a memory variable and/or assign the function block output to input of another function block and/or assign the function block output to relevant analog or digital out put from the system.
- Facilitates setting of page size, colors and Printing of the FBDs

Function Block Diagram of ECCS Logic



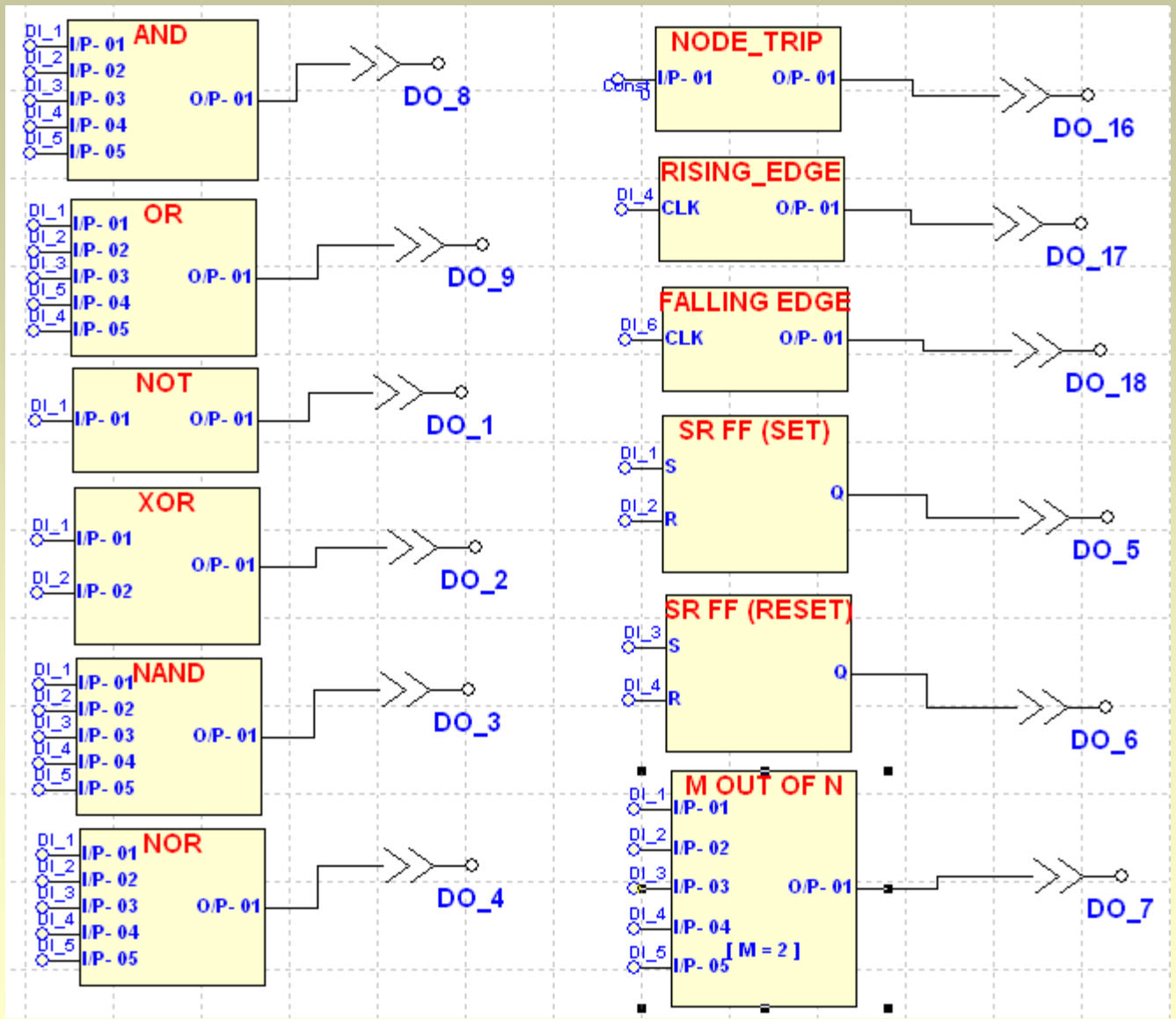


Function block Library

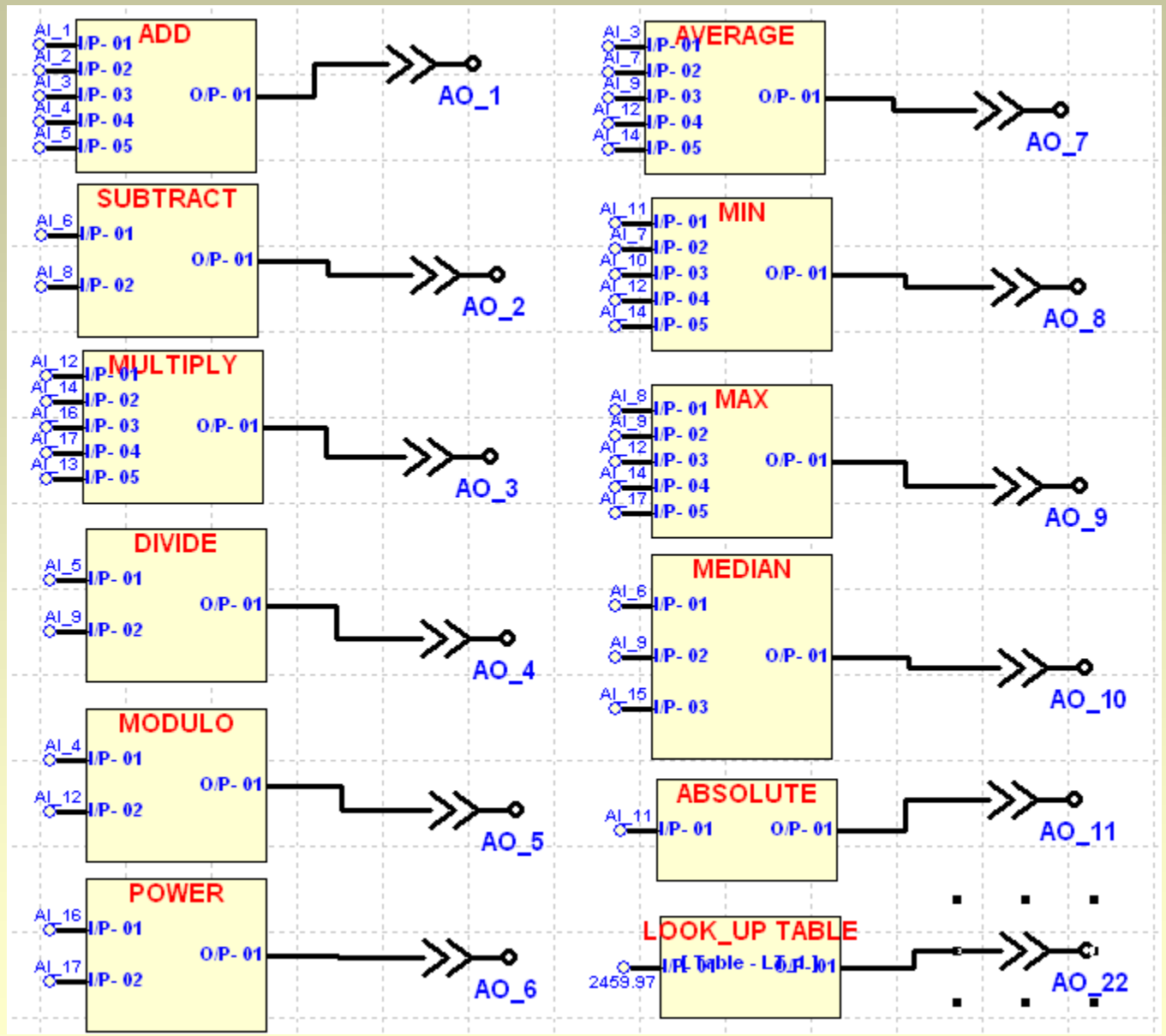
Phase 1 of TPLC-32 supports 61 function blocks categorized in to following types.

- Logical Function Blocks
- Arithmetic Function Blocks
- Selection and look-up table Function Blocks
- Comparison Function Blocks
- Timer function Blocks
- Counter function Blocks
- Alarm group Function Blocks
- Type Conversion Function Blocks
- Feed Back Function Blocks
- Trip function block

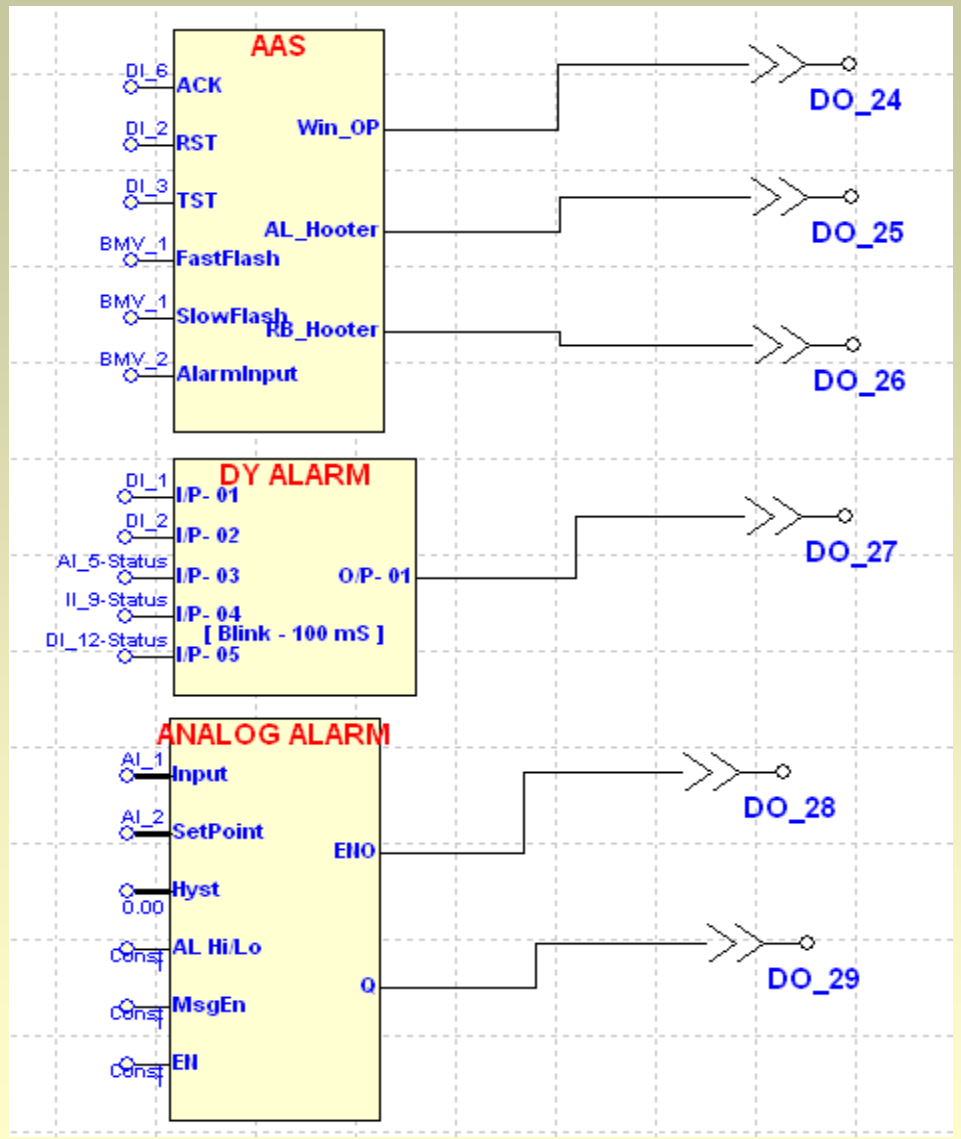
Logical Function blocks

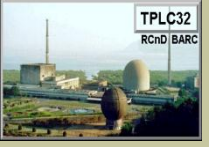


Arithmetic Function Blocks



Alarm Function Blocks

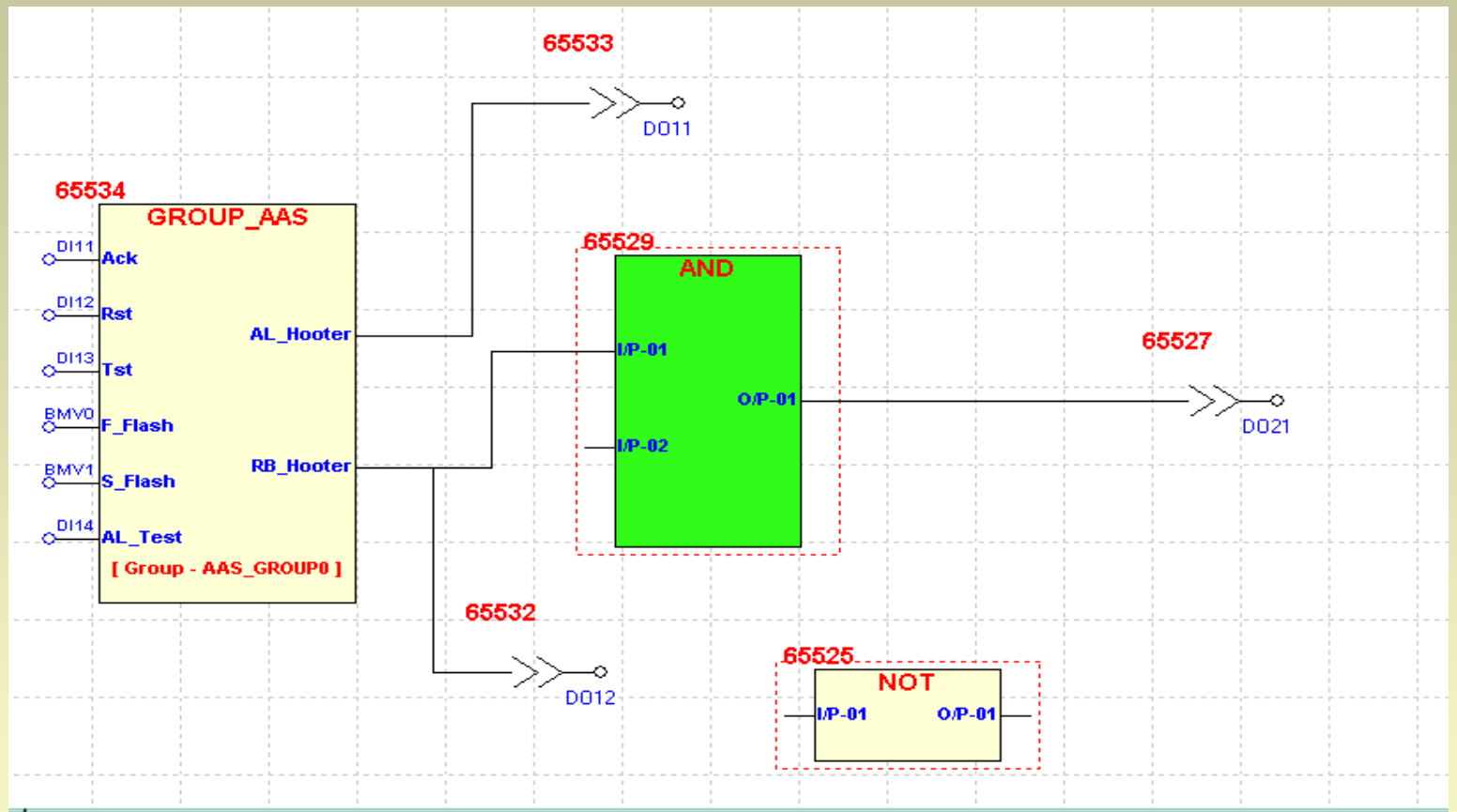




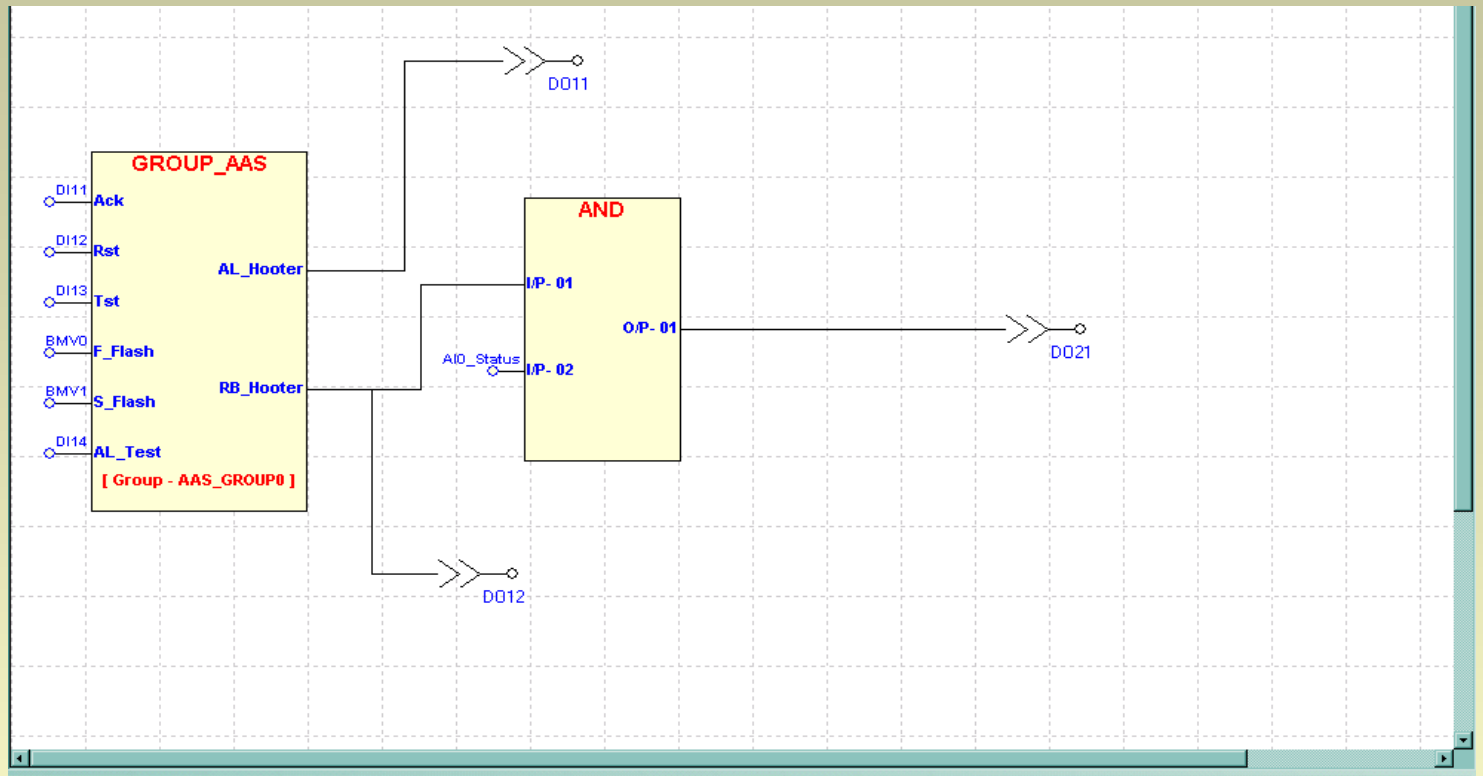
Application Build

- This option compiles the selected node in a project
- It checks for correctness of system configuration
- It checks for correctness of Application developed in the form of function block diagram.
- In case of any error in system configuration or FBDs , it identifies the error and halts build process.
- On successful build, it gives estimated cycle time of the application on target TPLC-32 hardware.
- For the successfully built application it facilitates, testing of the application locally with simulated inputs.

Screen Shot of error In System Build



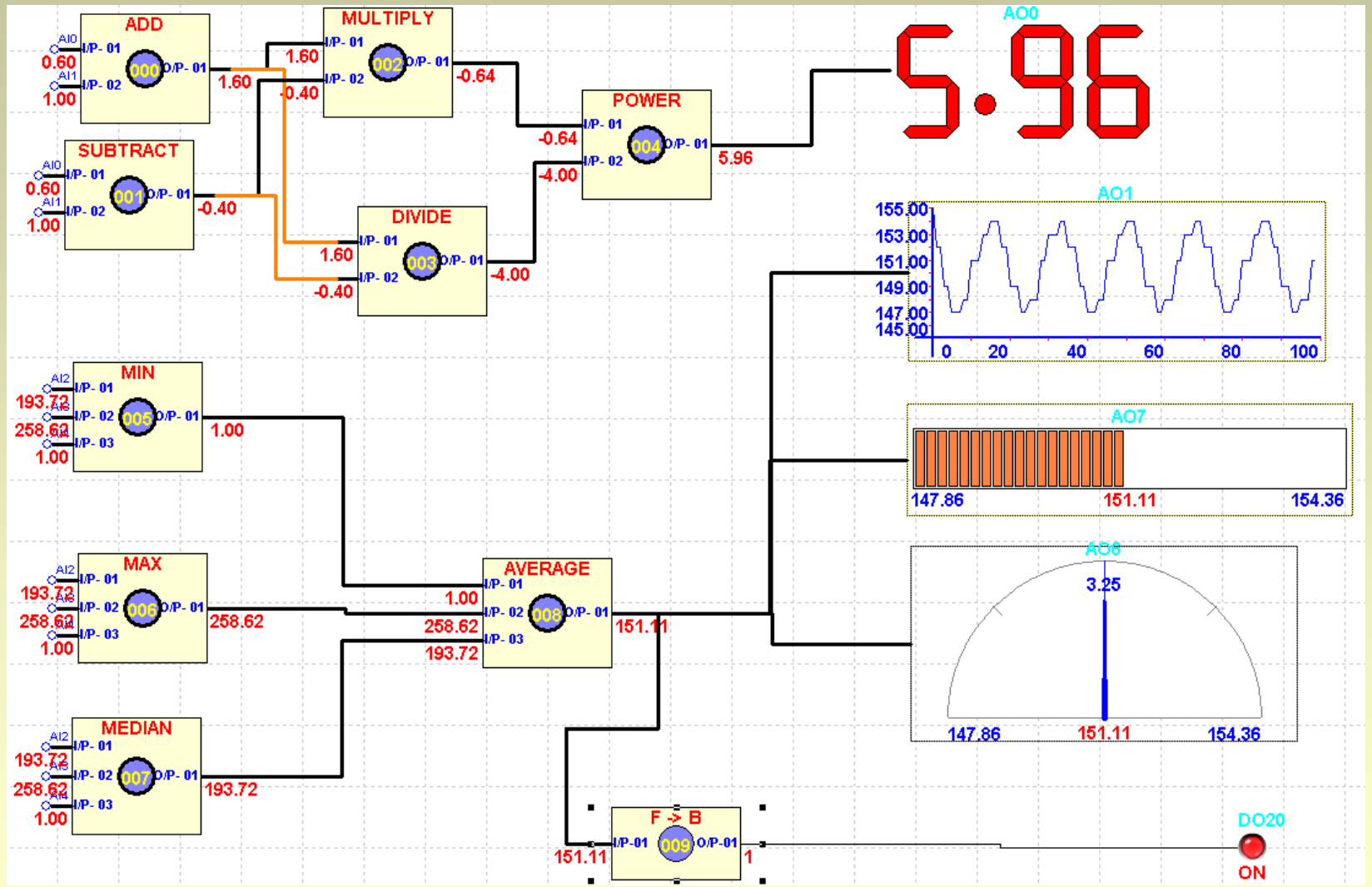
Screen Shot of Successful System Build



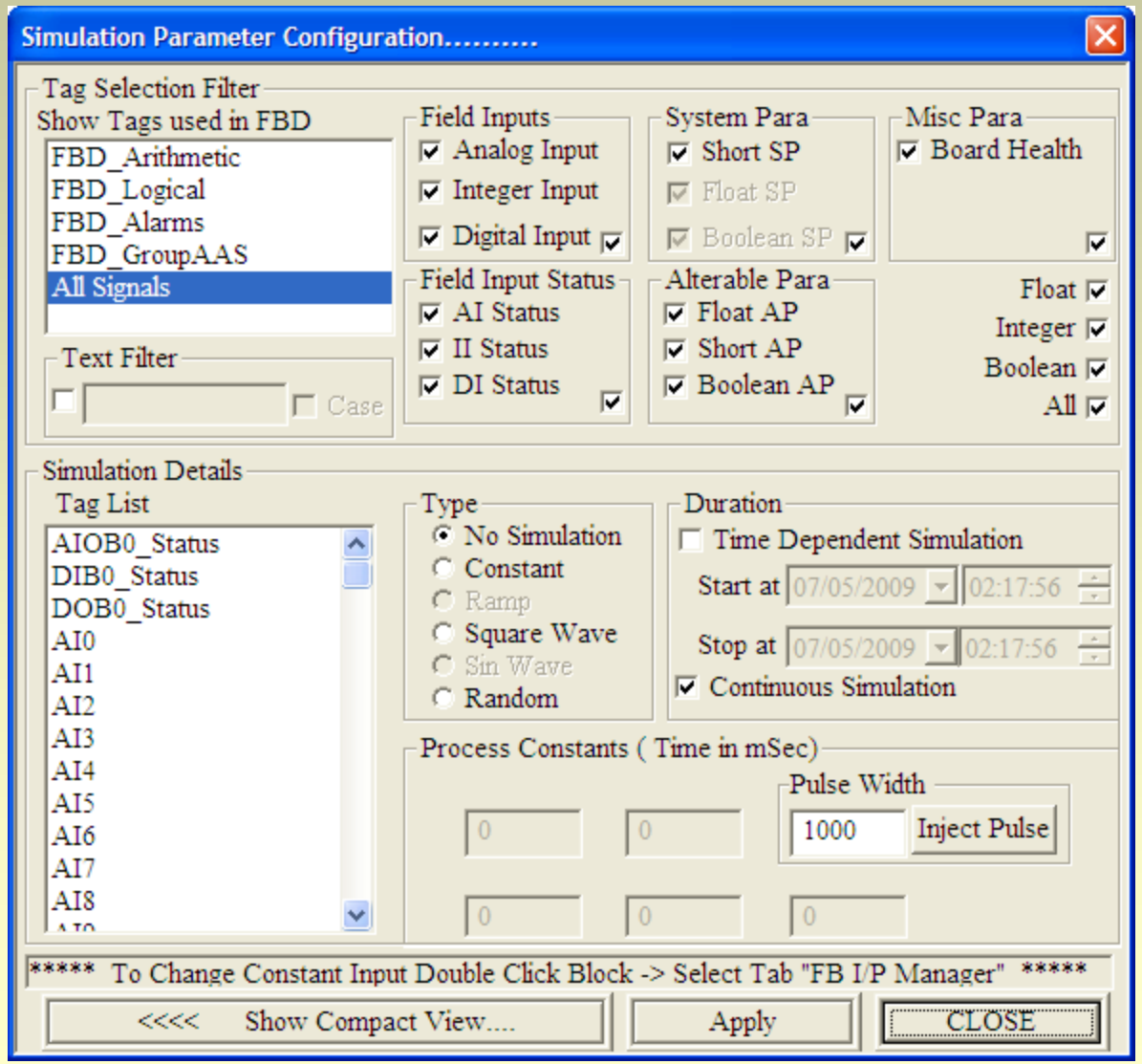
Output...

```
Build Started for - FBD_Arithmetic
Build Completed Successfully for above file.....
Build Started for - FBD_Logical
Build Completed Successfully for above file.....
Build Started for - FBD_Alarms
Build Completed Successfully for above file.....
Build Started for - FBD_GroupAAS
Build Completed Successfully for above file.....
Memory Variable analysis started.....
Memory Variable analysis Completed Successfully.....
Configuration Integration started........
Configuration Integration Completed Successfully........
Execution Time of control Task =    1.45 mSec
System Build for Node1 Successful....   :  10/08/2009 13:47:02
```

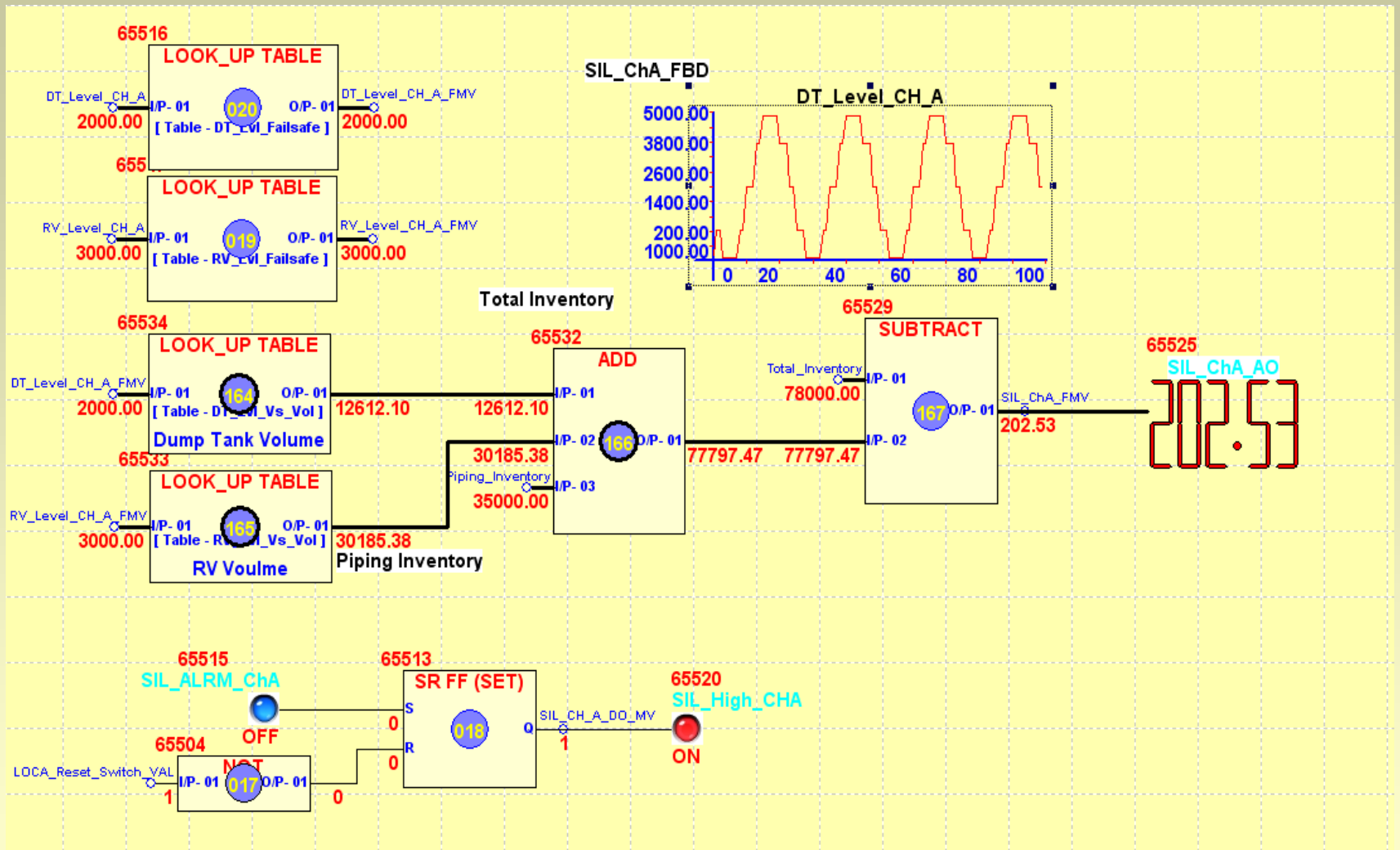
Screen Shot of off-line simulation

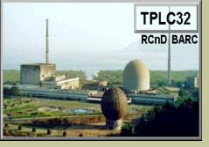


Off-line simulation Settings



Screen Shot of Run Time Debugging

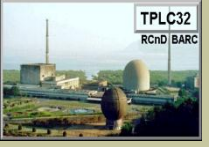




Systems Developed using TPLC-32 Platform

Following C&I Systems of Dhruva Research Reactor are developed using TPLC-32

- Reactor Trip Logic system (RTLS) Cycle Time 15 (8) mille seconds
- Reactor Startup Logic System (SULS) Cycle Time 10 (5) mille seconds
- Emergency Core cooling Logics (ECCS) Cycle Time 20 (8) mille seconds
- Alarm Annunciation System (AAS) Cycle Time 10 (7) mille seconds.
- Development of Distributed Control system for Integrated Project of NRB Based on TPLC-32 (Phase B) is in progress.



Salient Features RTLS of Dhruva

RTLS has Three channels, with limited local 2 out 3 (group concept) with majority voting logic

Inputs:

Absolute Trips

- Analog 4 – 20 mA (30)
- Digital potential free (72)

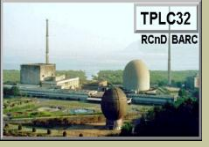
Conditional Trips

- Analog 4 – 20 mA (148)
- Digital potential free (90)

Outputs:

- Trip Ladder Circuit – 6
- Parameter trip window annunciation – 216
- Group trip – 96
- Annunciation through AAS – 18

Cycle Time of 15 mille seconds.



SULS and ECCS Systems of Dhruva

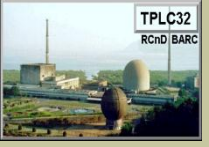
suls_ver0 -> SULS_CH_A

Name	Values
Name	SULS_CH_A
Des	NA
CycleTime	10
Version	1
No. of AIO Boards	0
No. of DI Boards	4
No. of DO Boards	0
No. of NW Boards	2
No. of RO Boards	3
No. of AI Tags	0
No. of II Tags	0
No. of AO Tags	0
No. of IO Tags	0
No. of DI Tags	89
No. of DO Tags	35
No. of Bool MV Tags	235
No. of Short MV Tags	0
No. of Float MV Tags	36
No. of Bool AP Tags	0
No. of Short AP Tags	7
No. of Float AP Tags	2
No. of Bool SP Tags	5
No. of Short SP Tags	10
No. of Float SP Tags	0
No. of Analog Alarm Tags	34
No. of Digital Alarm Tags	234
No. of Int Alarm Tags	0
No. of AASGroup Tags	0
No. of Look UP Tables	0
No. of Function Blocks	0
No. of Network Connections	3
No. of Network DataPackets	5
No. of Network MapPacketToConnection	5

Dhruva_ECCS_27_04_2011_0_0 -> ECCS_Channel_A

Name	Values
Name	ECCS_Channel_A
Des	ECCS
CycleTime	20
Version	0
No. of AIO Boards	2
No. of DI Boards	5
No. of DO Boards	0
No. of NW Boards	2
No. of RO Boards	5
No. of AI Tags	56
No. of II Tags	0
No. of AO Tags	5
No. of IO Tags	0
No. of DI Tags	160
No. of DO Tags	80
No. of Bool MV Tags	90
No. of Short MV Tags	0
No. of Float MV Tags	51
No. of Bool AP Tags	0
No. of Short AP Tags	1
No. of Float AP Tags	4
No. of Bool SP Tags	5
No. of Short SP Tags	10
No. of Float SP Tags	0
No. of Analog Alarm Tags	140
No. of Digital Alarm Tags	217
No. of Int Alarm Tags	0
No. of AASGroup Tags	0
No. of Look UP Tables	13
No. of Function Blocks	296
No. of Network Connections	1
No. of Network DataPackets	2
No. of Network MapPacketToConnection	2

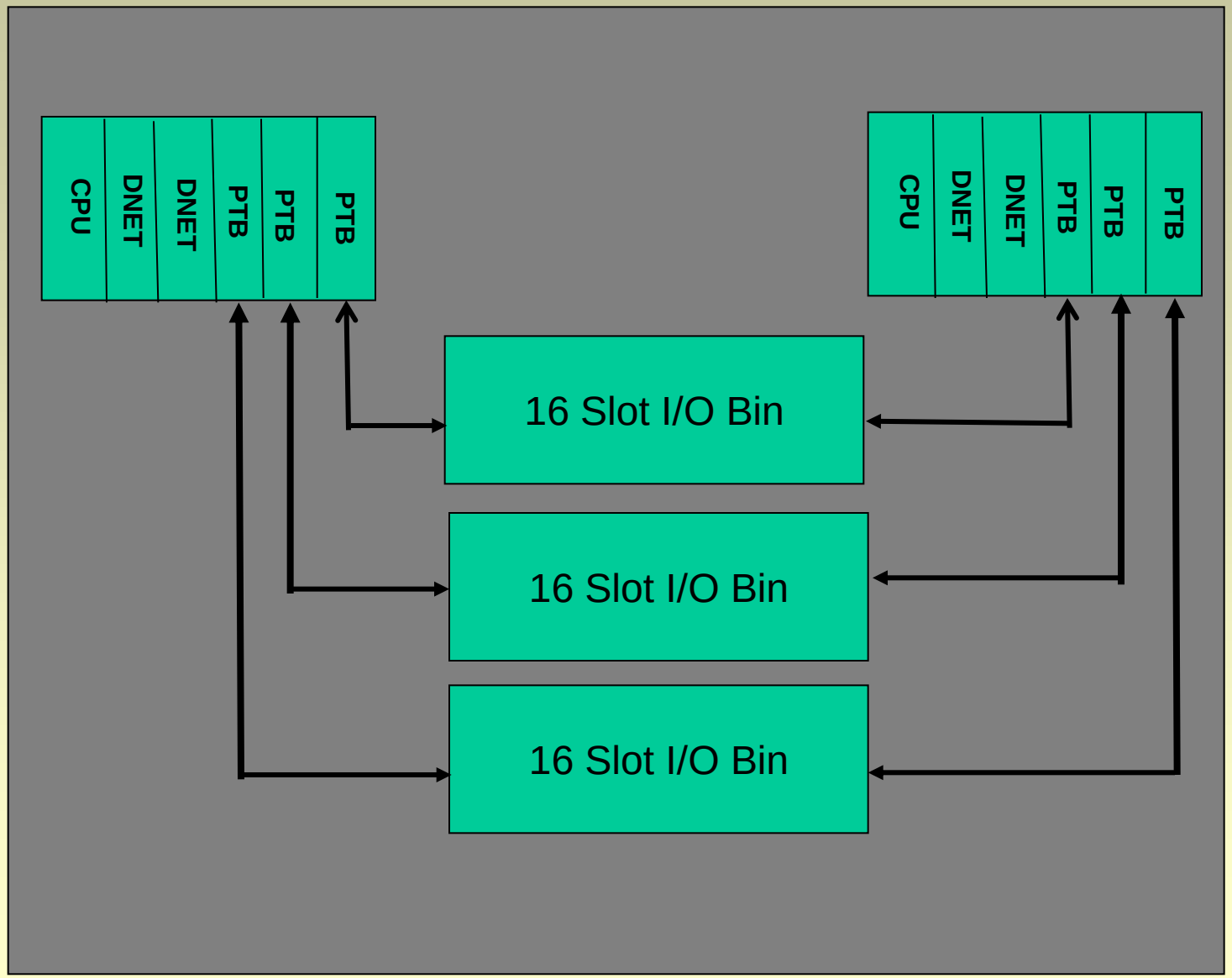
TPLC-32 Based Alarm Annunciation System of Dhruva



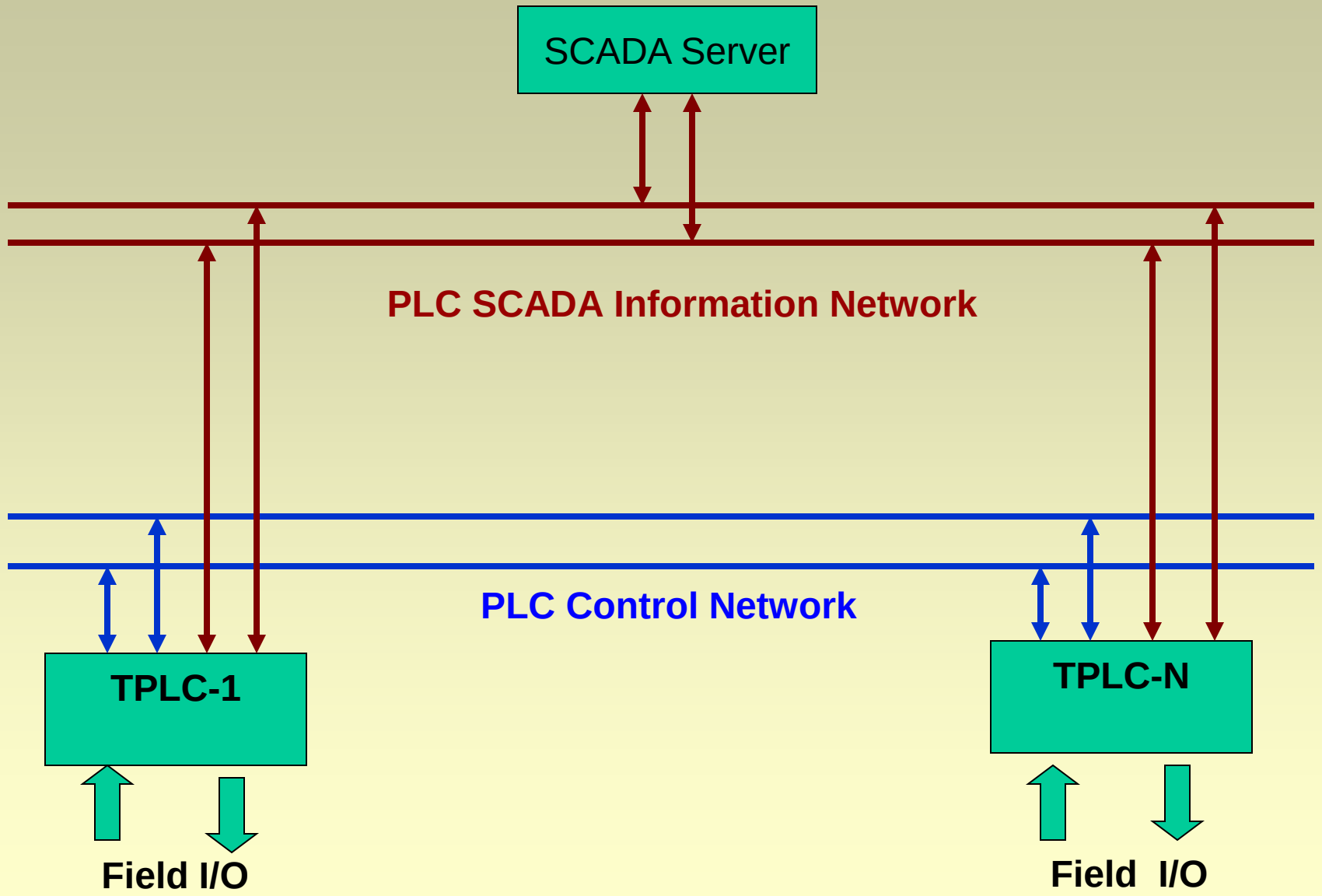
Further Enhancements in TPLC-32

- TPLC Design with Dual Redundant Hot standby CPU
- Configuration of Distributed PLC Architecture
- Support for Networked I/O
- Function block library supporting about 200 function blocks
- Super block i.e. User defined function block build from library of existing function blocks
- Provision to accept supervisory control commands over network from soft consoles / SCADA Stations
- MOD BUS and OPC connectivity for seamless integration with COTS SCADA packages

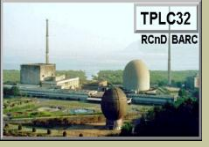
DUAL CPU Based TPLC-32



Architecture of Distributed Control system Based on TPLC-32



TPLC-32 based prototype DCS



New function Blocks and Super Block

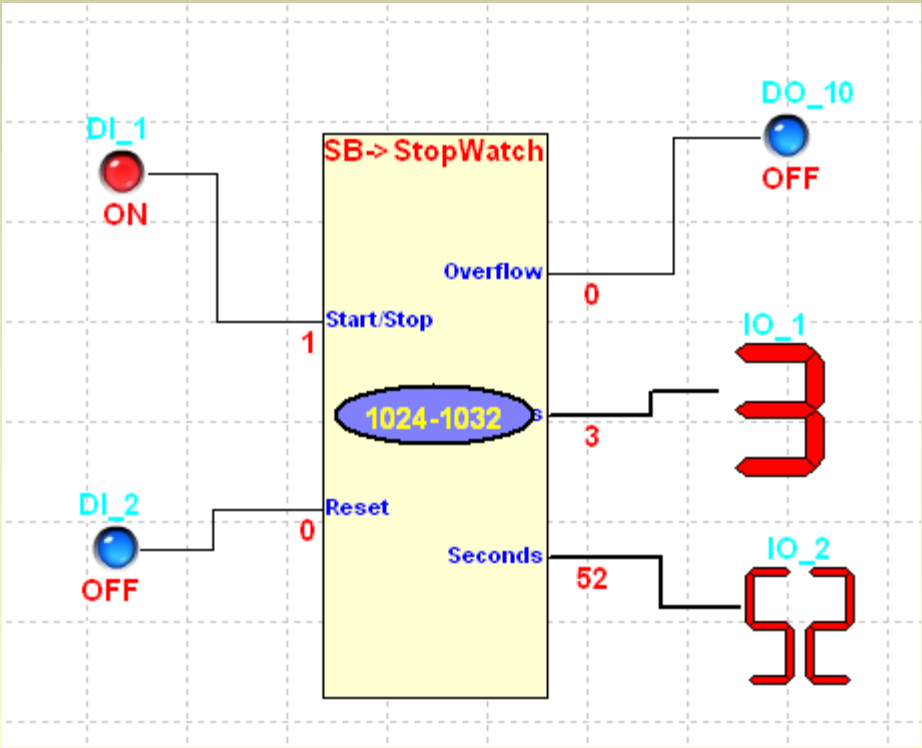
New Function Blocks:

- PI, PD, PID function Blocks
- **Range Converter Function Blocks**
- Sequencer Function Block
- **Signal generator function blocks**
- Type converter and buffer blocks

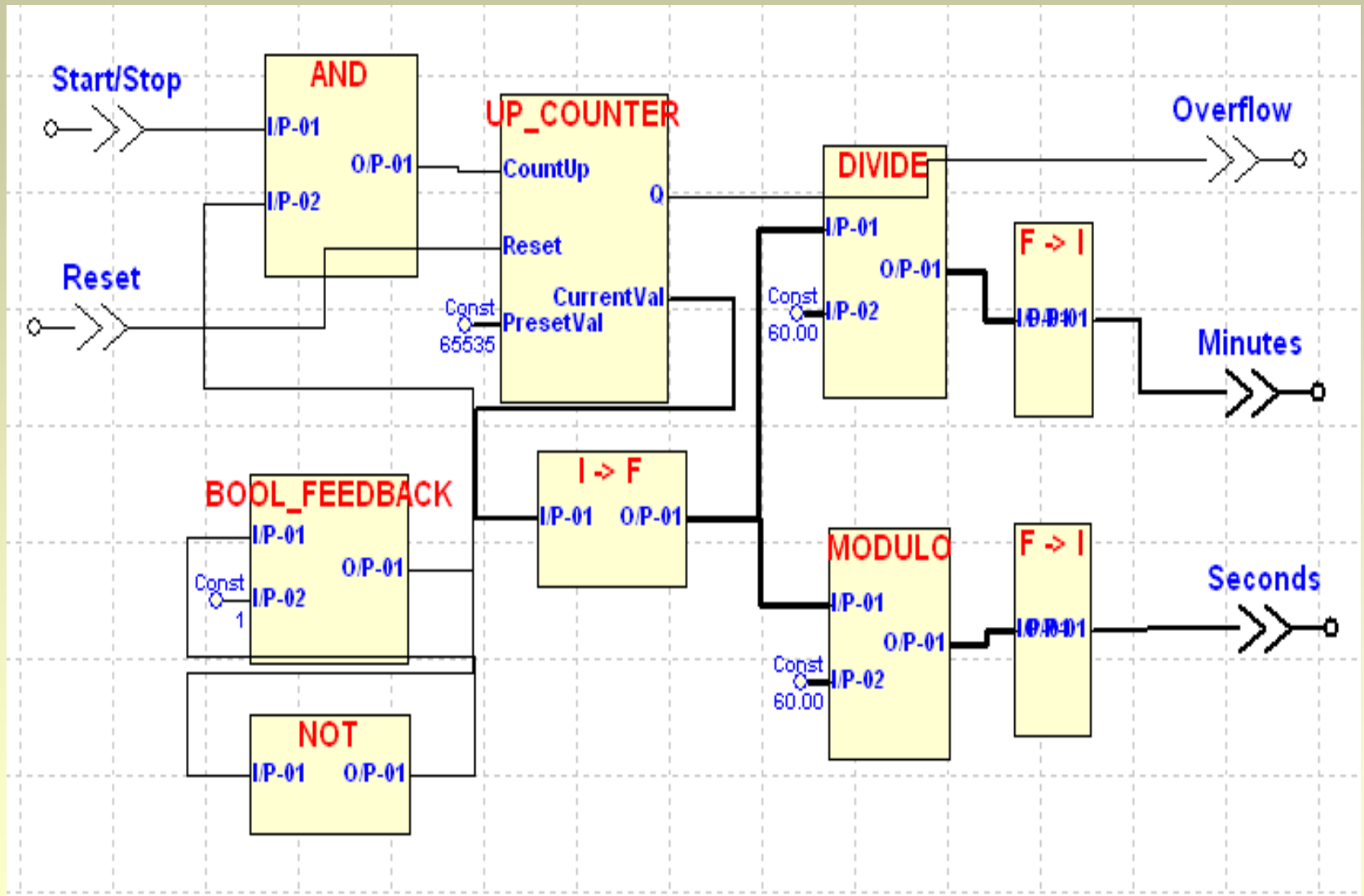
Super Block:

- Super blocks are User defined function blocks.
- **Super blocks are developed by user using existing standard function blocks available in the platform**

Super Block: Stop Watch



In side Stop Watch



Acknowledgements

- TPLC-32 Software Development Team Members
- Members of EHS Hardware Design Team
- Members of Independent V&V team
- System Developers and Testers
- Head, Reactor Control Division, BARC
- Associate Director , E&I Group ,BARC
- Director , E&I Group, BARC

Thanks for Your Attention