FPGA BASED HIGH SPEED DATA ACQUISITION CARD

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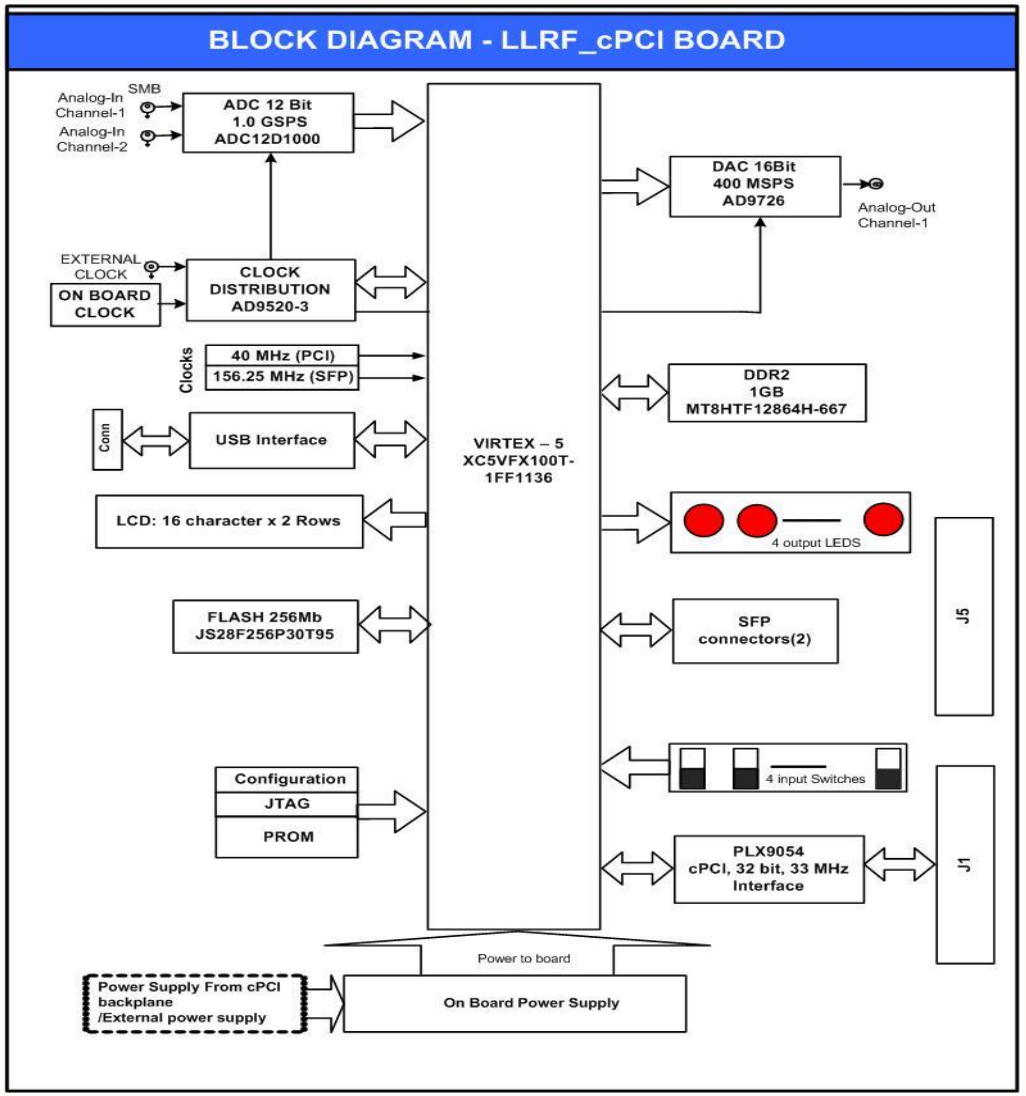
Plan of Talk:

- Features and functionality
- Salient design issues
  - I/O Budget
  - PCB design (Package delay, PCB delay, I/o banking issues)
  - ADC features (Different modes, ADC clock, FPGA primitives)
- Applications
  - LLRF
  - Pulse acquisition
- Results
- Conclusions

Features & functionality :

- Card form factor: 6U
- Two on-board 12 bit analog input channels that can digitize at a maximum effective sampling rate of 1000 Msps.
- On-board 16 bit 400 Msps DAC
- On-board 2GB DDR2 RAM
- On-board 32 bit, 33 MHz PCI interface
- On-board high speed interface for fast data transfer to PC
    - Two SFP connectors each having a speed of 1.5 Gbps
- On-board USB interface
- On-board clocks:
    - 100 MHz clocks for ADC/DAC given to clock distribution IC
    - 40 MHz clock for PCI interface.
    - Facility to accept external clock input
- TTL compatible trigger inputs.
- Input power connector.
- On-board FPGA (Virtex 5) and PROM
- Configuration through JTAG

System Block Diagram



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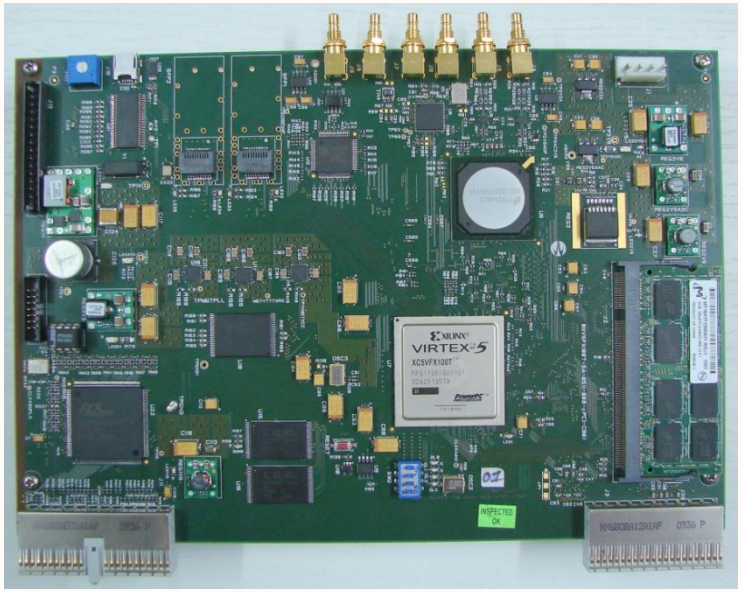

Data is sampled by the ADC, stored in the DDR2 memory. This memory is then read and the data is processed according to the relevant algorithms typical to the application being developed. The processed data is then transferred to the PC via the cPCI link.

Card has been designed to function as a platform (either stand-alone or chassis based) for developing and evaluating different FPGA based hardware designs.

Salient design issues:

I/O BUDGET

IO CALCULATION								
Board_Name:- LLRF cPCI Card								
No. Of Chips	Main Device	COMPONENT NAME	No. of I/Os Available	I/Os Per Chip	Total I/Os Used	Supply Voltage	Available I/Os	Number of banks required
	Virtex - 5	**FX100T - 1136**	**640**				**81**	
1	ADC	ADC12D1000		106	106	2.5V		3 X 40
1	ADC	ADC12D1000		15	15	1.8V		1 X 20
1	DDR 2	MT16HTF25664H-667		160	160	1.8V		4 X 40
1	DAC	AD9726		36	36	2.5V		2 X 40
1	DAC	AD9726		5	5	3.3V		4 X 40
1	USB	CY7C68013A		26	26	3.3V		
2	SFP Connector	SFP Connector		2	4	3.3V		
1	4 DIP Switches	4 DIP Switches		4	4	3.3V		
1	4 Output LEDs	4 Output LEDs		4	4	3.3V		
1	LCD			11	11	3.3V		
1	cPCI			60	60	3.3V		
1	Clock Generator	AD9520-3		13	13	3.3V		
1	Vrp , Vrn			28	28			
1	Differentail Clock				0	2.5V		1X20
1	Flash	JS28F256P30T95		49	49	3.3V		
1	Single ended clock				0	3.3V		1X20
1	PROM data lines			8	8	3.3V		1X20
1	Free Ios			30	30	3.3V		1X40
					559			

Salient design issues

- Channel delays play a significant role in determining the overall phase difference

- **Package delay** is the time required to propagate from I/O buffer to I/O pad
- **PCB delay** is the interconnect delay involved due to PCB routing and placement
- The overall path delay should be equal for samples to reach FPGA without any loss
- Hence care must be taken to optimize this delay, thereby, increasing accuracy level of data acquisition.

- Delay matching techniques –

1. To minimize the package delay, we try to accommodate all output pins of the ADC to those FPGA I/O banks which are either in same clock region or quite adjacent clock regions.
2. During synthesis, the FPGA logic is placed near to that clock region in which, I/O banks incorporating the interface ports are present. This reduces the **package delay** and also improves on **Clock Skew.**
3. Any slight variation in the package delay is compensated in the PCB delay so as to obtain a uniform **net path delay.**

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IO BANKING DIAGRAM VIRTEX – 5 FX100T 1136

<table>
<tr>
<td>Bank – 0
No.of IO - 20
VCCIO = 3.3V
PROM</td>
<td>Bank – 20
No.of IO - 40
VCCIO = 3.3V
FLASH,LCD,
USB</td>
<td>Bank – 12
No.of IO - 40
VCCIO = 3.3V
FLASH</td>
<td>Bank – 5 No. of IO - 40
VCCIO = 3.3V
DAC ,USB,
SYNTH,SFP

Bank – 3 No. of IO - 20
VCCIO = 2.5V
DAC_CLK , ADC_CLK

Bank – 1 No. of IO - 20
VCCIO = 1.8V
ADC
DC</td>
<td>Bank – 23
No.of IO - 40
VCCIO = 2.5V
DAC</td>
<td>Bank – 19
No.of IO - 40
VCCIO = 2.5V
ADC</td>
<td>Bank – 15
No.of IO - 40
VCCIO = 2.5V
ADC</td>
<td>Bank – 11
No.of IO - 40
VCCIO = 2.5V
ADC</td>
</tr>
<tr>
<td colspan="3">Bank – 18 No. of IO - 40
VCCIO = 3.3V
cPCI

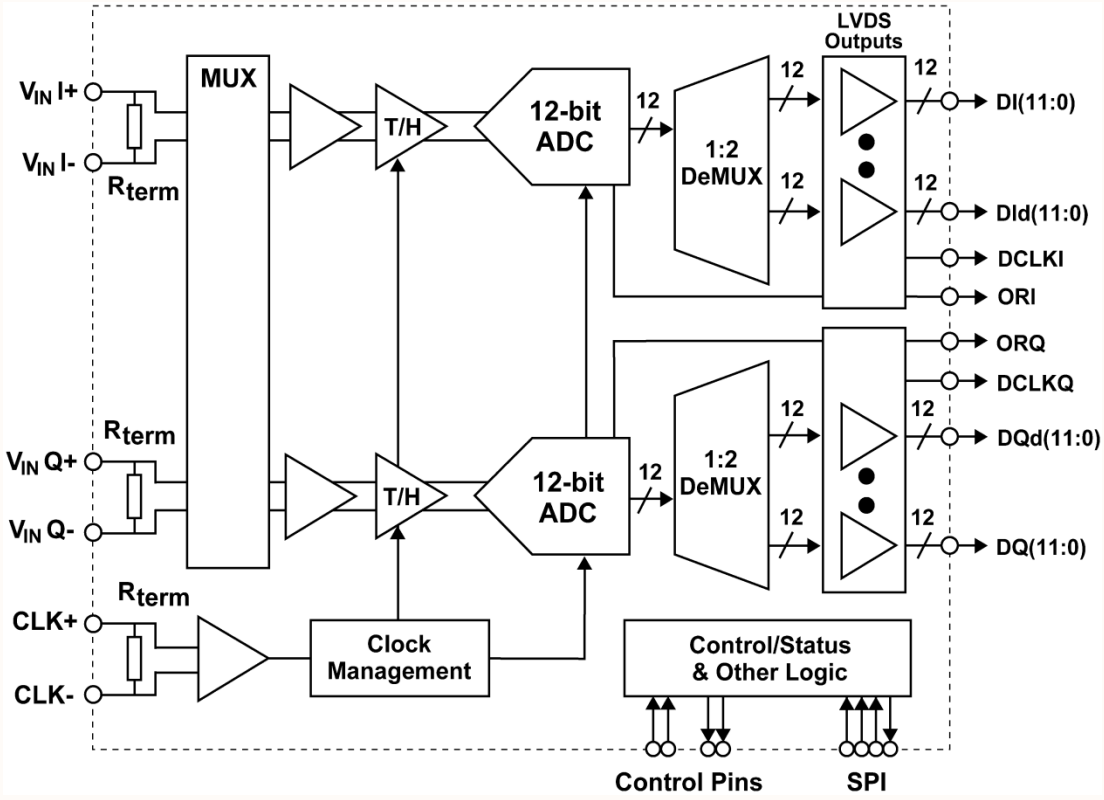
Bank – 22 No. of IO - 40
VCCIO = 3.3V
cPCI,switches , LED</td>
<td>Bank – 2 No. of IO - 20

Bank – 4 No. of IO - 20
VCCIO = 3.3V
DDR2_CLK

Bank – 6 No. of IO - 40
VCCIO = 3.3V
FREE IOs</td>
<td>Bank – 25
No.of IO - 40
VCCIO = 1.8V
DDR2</td>
<td>Bank – 21
No.of IO - 40
VCCIO = 1.8V
DDR2</td>
<td>Bank – 17
No.of IO - 40
VCCIO = 1.8V
DDR2</td>
<td>Bank – 13
No.of IO - 40
VCCIO = 1.8V
DDR2</td>
</tr>
</table>

ADC Features

- Single supply operation
- Test pattern outputs for debugging
- Internal Calibration Feature sets internal bias currents which affect the linearity of the converter. This minimizes full-scale error, offset error, DNL and INL, which results in the maximum dynamic performance, as measured by: SNR, THD, SINAD (SNDR) and ENOB.
- Availability of output clock to latch data
- Different operating modes: DES, Non-Des, Demux, Non-Demux modes



ADC modes:

DES/Non-DES Mode

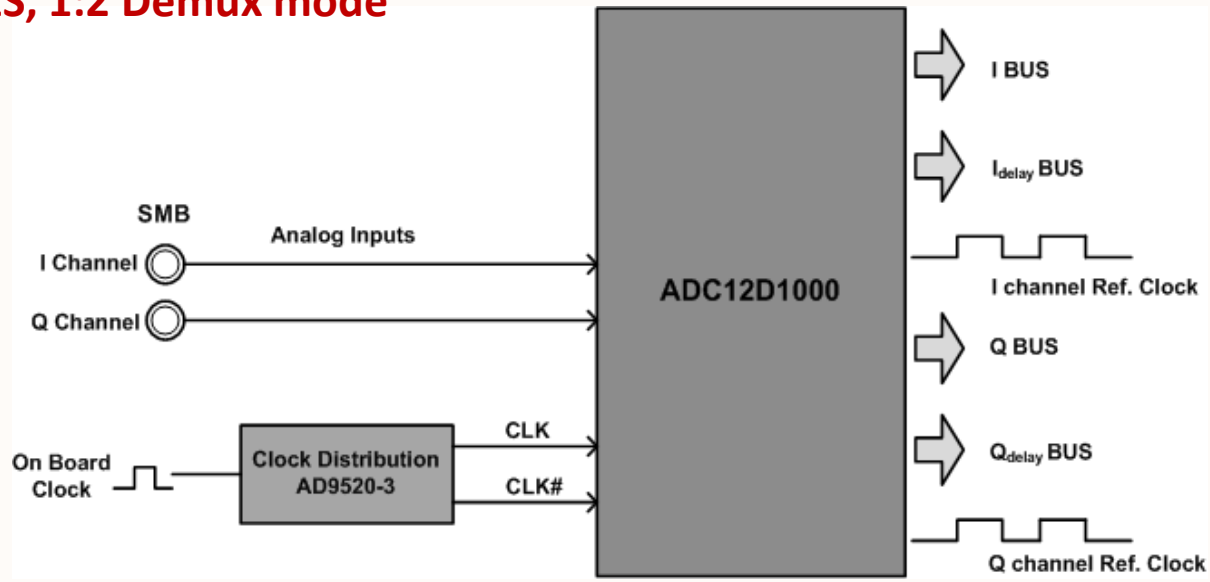
The ADC can operate in Dual-Edge Sampling (DES) or Non-DES Mode. The DES Mode allows for a single analog input to be sampled by both I- and Q-channels. One channel samples the input on the rising edge of the sampling clock and the other samples the same input signal on the falling edge of the sampling clock. A single input is thus sampled twice per clock cycle, resulting in an overall sample rate of twice the sampling clock frequency, e.g. 2.0 GSPS with a 1.0 GHz sampling clock.

Demux/Non-demux Mode

The ADC12D1000/1600 may be in one of two demultiplex modes: Demux Mode or Non-Demux Mode (also sometimes referred to as 1:1 Demux Mode). In Non-Demux Mode, the data from the input is simply output at the sampling rate on one 12-bit bus. In Demux Mode, the data from the input is output at half the sampling rate, on twice the number of buses. Demux/Non-Demux Mode may only be selected by the NDM pin. In Non-DES Mode, the output data from each channel may be demultiplexed by a factor of 1:2 (**1:2 Demux Non-DES Mode**) or not demultiplexed (**Non-Demux Non-DES Mode**). In DES Mode, the output data from both channels interleaved may be demultiplexed (**1:4 Demux DES Mode**) or not demultiplexed (**Non-Demux DES Mode**).

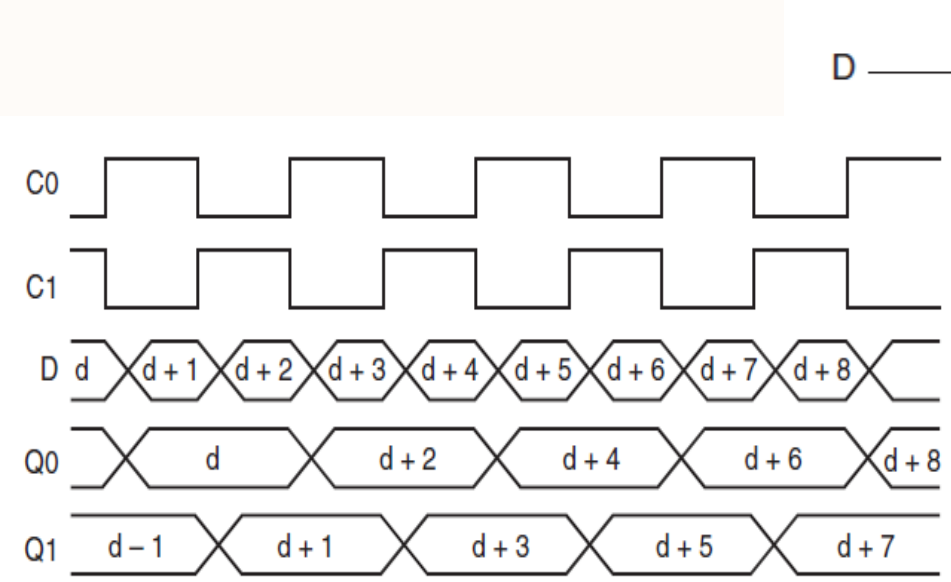
The ADC output data is always delivered in Double Data Rate (DDR). With DDR, the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK

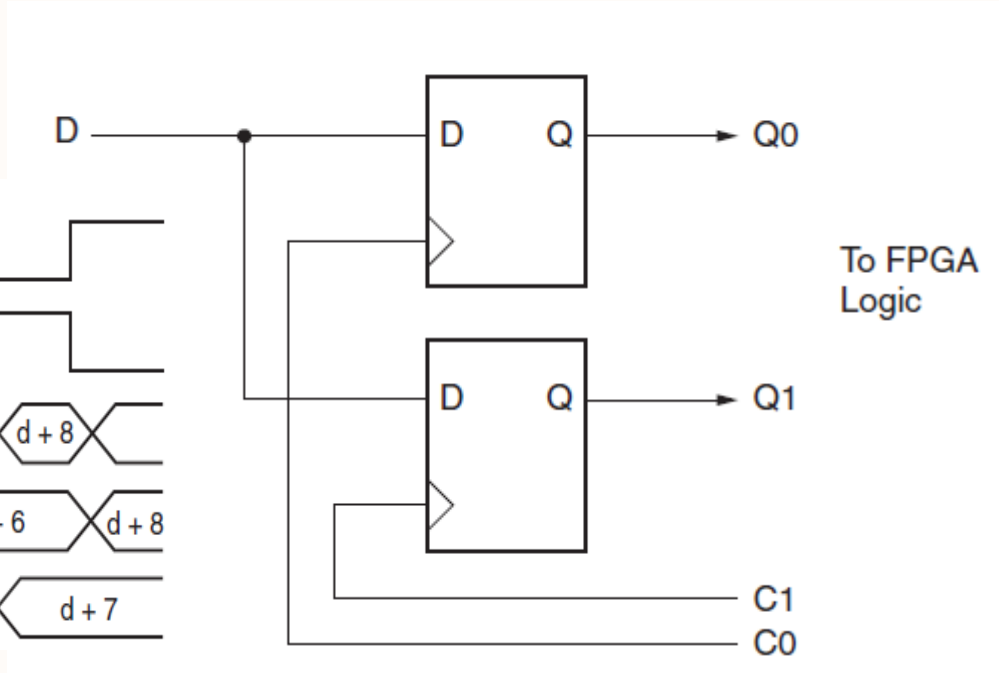
Non-DES, 1:2 Demux mode



- ADC is operating in DEMUX mode, i.e. it sends samples on two buses, I & I_{delay} for I channel and Q & Q_{delay} for Q channel.
- DDR data is coming to FPGA at a frequency of 250 MHz on two parallel Buses.
- I/O primitives are used to enable data acquisition.

- IDDR (Input Double Data Rate Register)
  - Converts the incoming DDR samples to SDR samples, thereby reducing the effective frequency of operation to half.

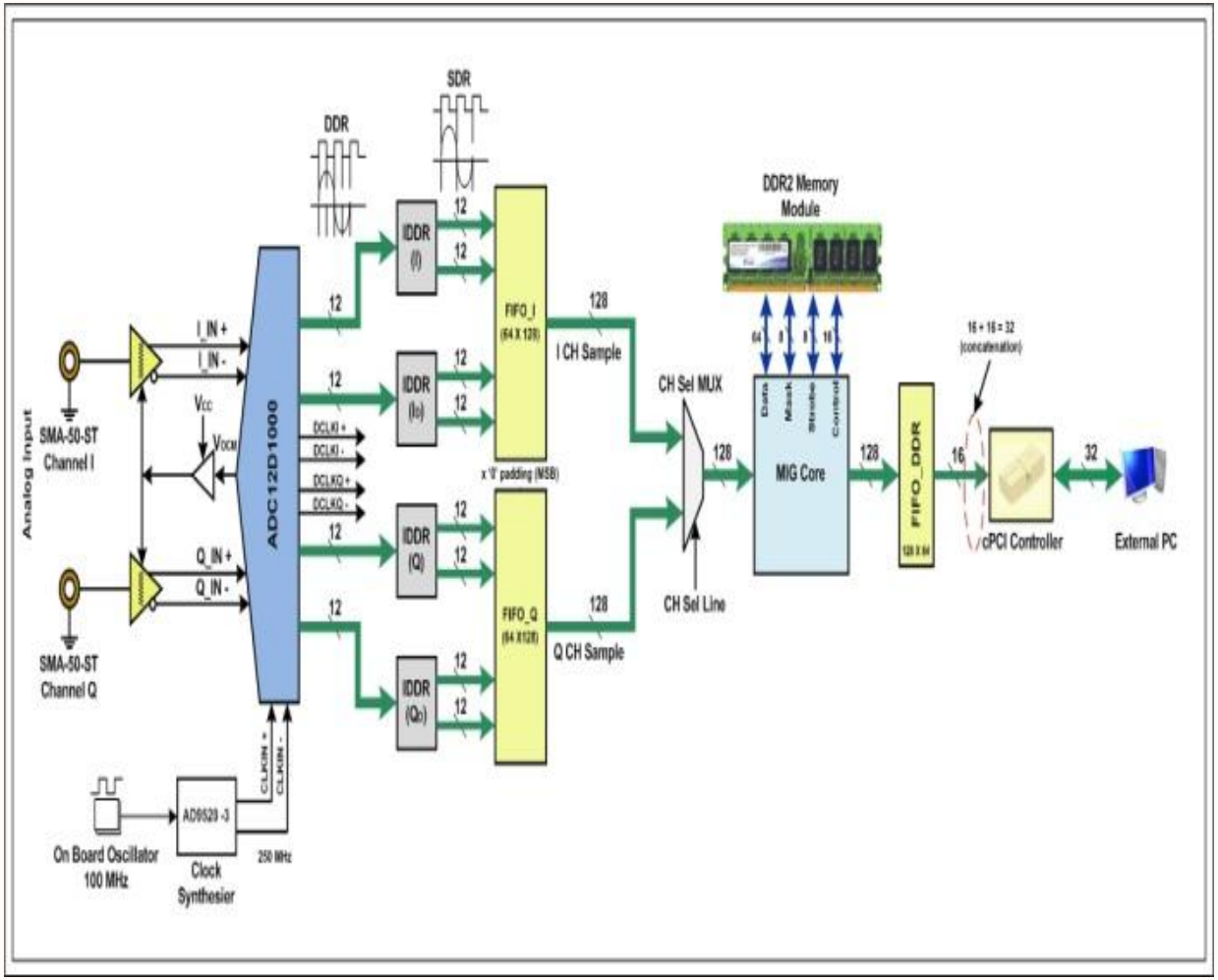




Salient design issues

The data acquisition hardware design consists of the following hardware entities:

- Configuration and calibration of external clock synthesizer (AD9520 -3)
- Configuration of ADC (ADC12D1000)
- Data acquisition of digital samples within the FPGA.
- Sample rearrangement and concatenation for writing to DDR2
- Write operation to DDR2 memory via Memory Interface Generator (MIG) core.
- Read operation from DDR2 memory via MIG core
- Rearrangement of samples to obtain the final stream of digital samples.
- Transferring data via cPCI interface.



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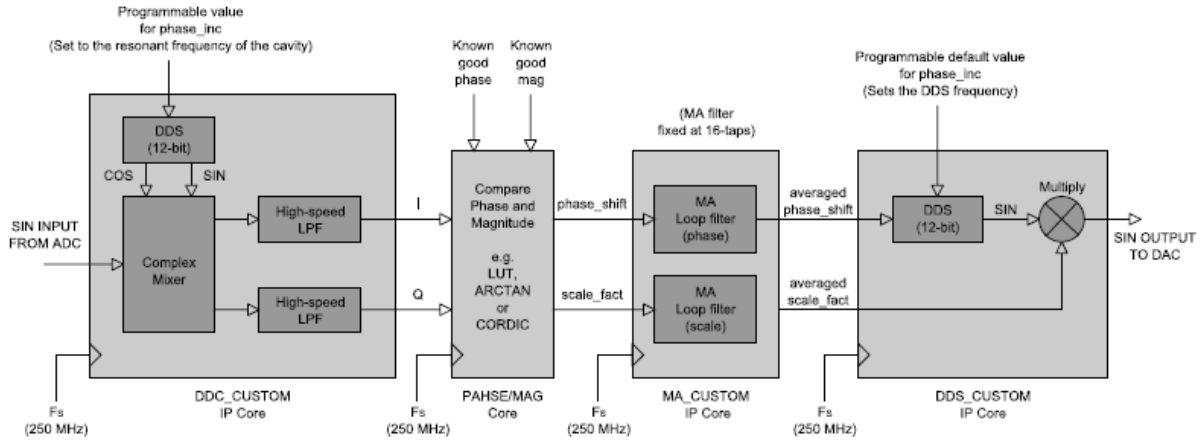
MA_CUSTOM IP Core

This IP Core acts as a loop-filter. It's purpose is to prevent abrupt changes to the *phase_shift and scale_fact* signals which may cause instability or oscillation in the loop. A simple moving-average filter has been implemented with 16-taps. The number of taps is currently fixed, but we can modify this if necessary. The moving-average filter also has the secondary effect of being a low-pass filter.



DDC_CUSTOM IP Core

This IP Core performs the digital mix-down of the IF input signal to baseband. It also generates the internal I/Q samples. The *phase_inc value controls the internal DDS frequency and should be set to the resonant frequency of* the cavity. Assuming a resonant frequency of ~75 MHz, then after the digital mix-down then this will generate tones at DC (75-75) = 0 Hz and also at 75+75 = 150 MHz. At clock rate of 250 MHz then the unwanted secondary tone at 150 MHz will also have an alias at 100 MHz (250-150). To this end, the FIR low-pass filters have been designed to block any frequency above 25 MHz.

DDS_CUSTOM IP Core

This DDS IP Core generates the output sinusoid waveform. The core uses a 12-bit LUT and has a programmable *phase_inc input that controls the frequency of the output sinusoid.*

The component also has additional *phase_shift and scale_fact inputs that can control the relative phase and* amplitude of the output signal.

The *phase_shift input is a 32-bit unsigned value. The full 32-bits represent a shift of 360°.*

The *scale_fact input is a 16-bit scale factor that scales the output waveform. It is a signed value in s1.14 format.*

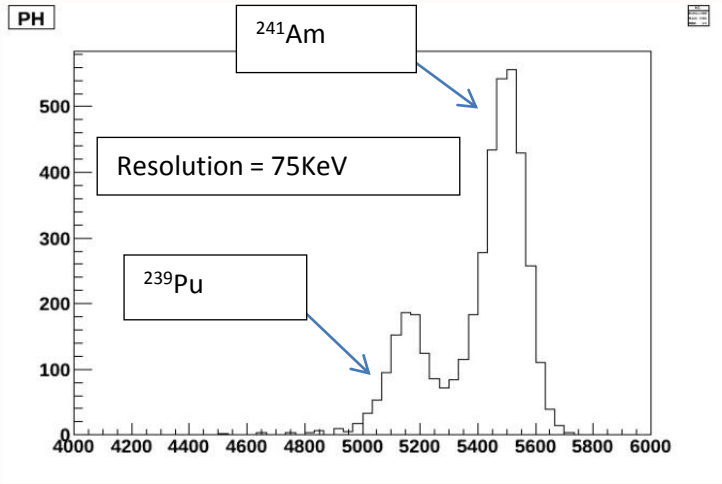
PHASE & MAGNITUDE COMPARATOR

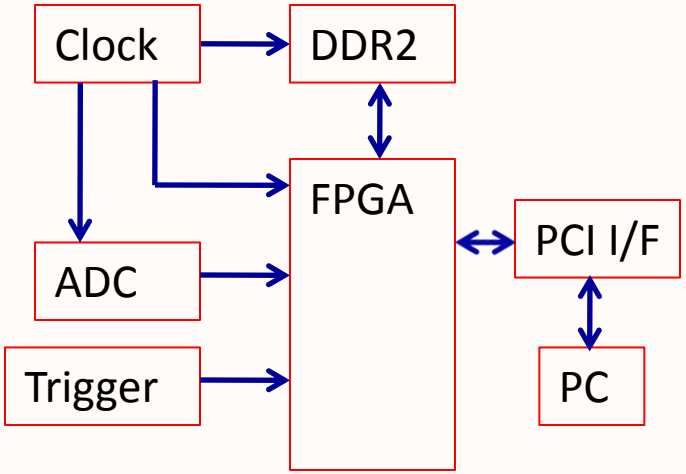
The PMC entity generates a known good phase and amplitude from the detected I and Q components. This is done Look-up-Table approach. The output of this entity is the phase and amplitude scale factor information.

Pulse Acquisition:

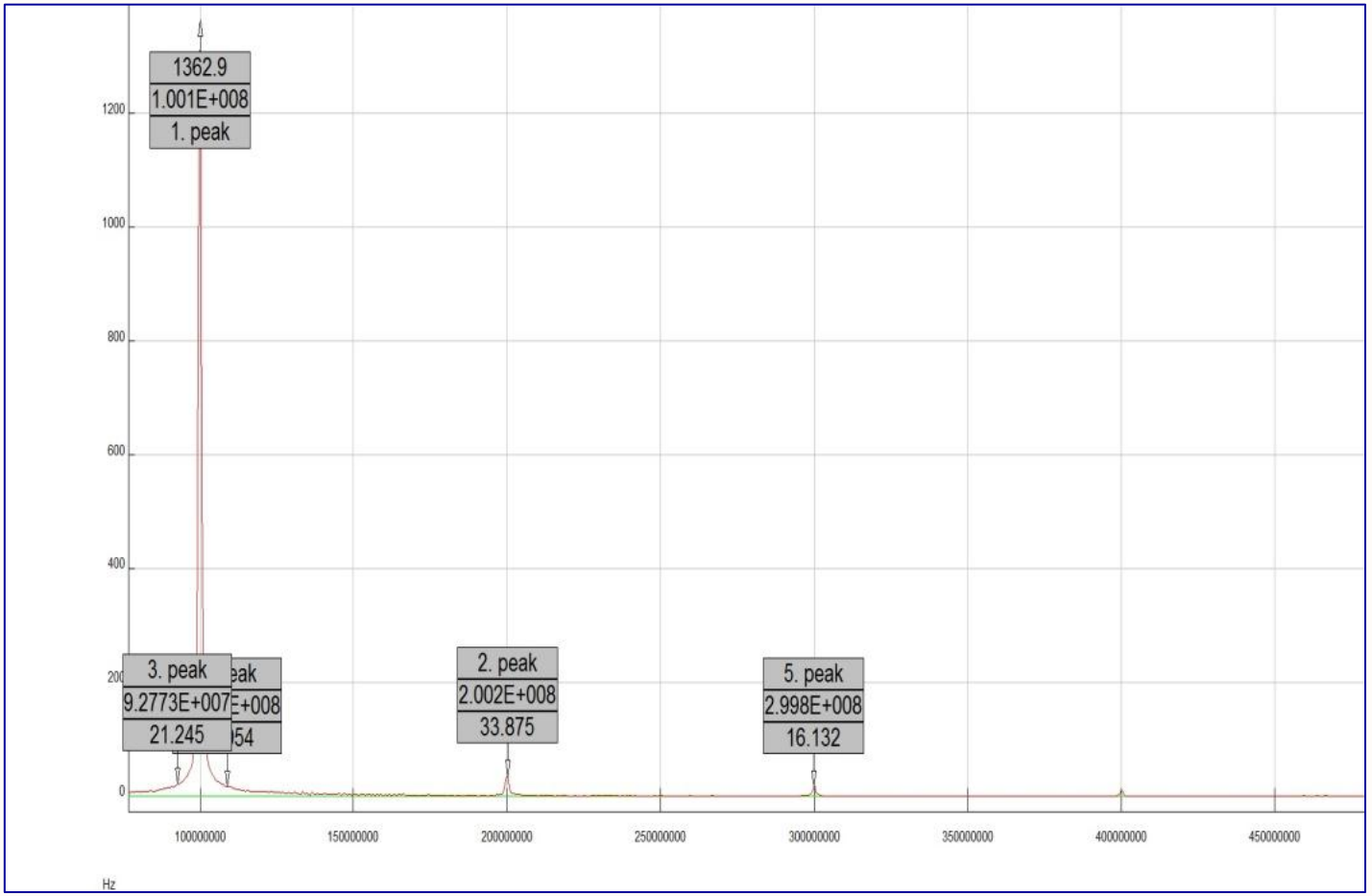
Pulses from surface barrier and silicon strip detectors were acquired at an input sampling rate of 1 Gs/s employing ^{241}Am and Am-Pu sources.

Amplitude spectrum generated in a offline mode after acquiring 2GB of data Data is acquired in a programmable pre-trigger mode implemented in FPGA.





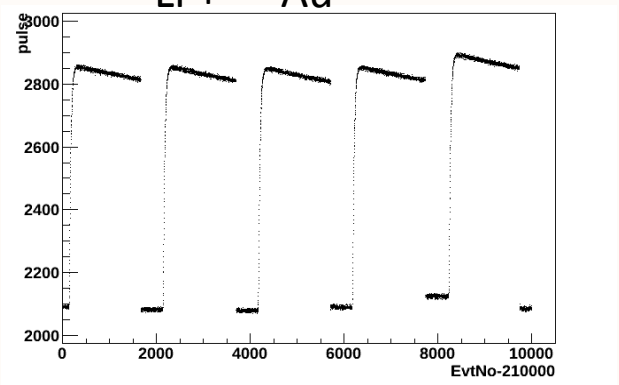
Results:


1362.9
1.001E+008
1. peak
3. peak
9.2773E+007
21.245
2. peak
2.002E+008
33.875
5. peak
2.998E+008
16.132
1200
1000
800
600
400
0
100000000
150000000
200000000
250000000
300000000
350000000
400000000
450000000
Hz

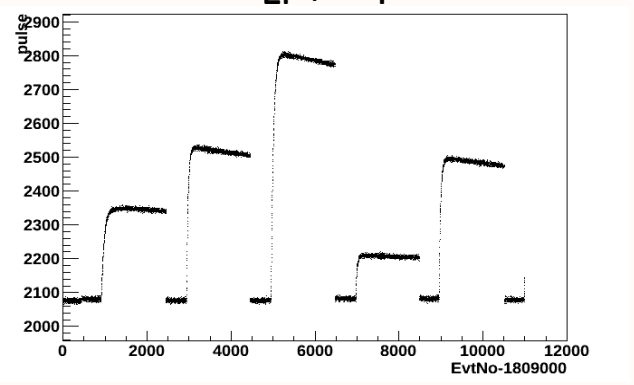
Latest Results:

Pulses from Preamplifier

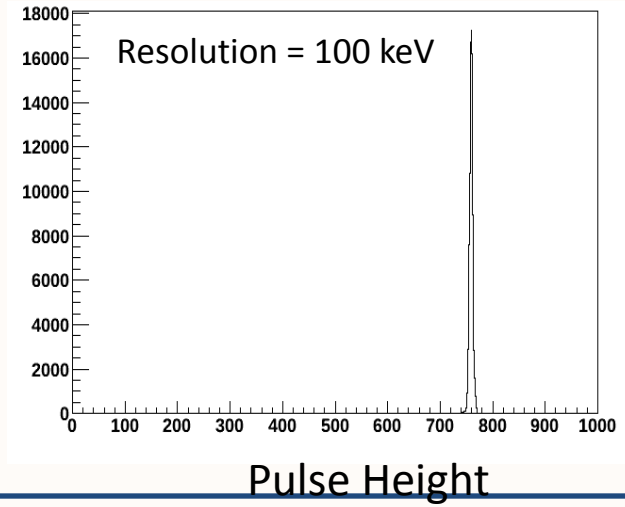
$^{7}Li + ^{197}Au$

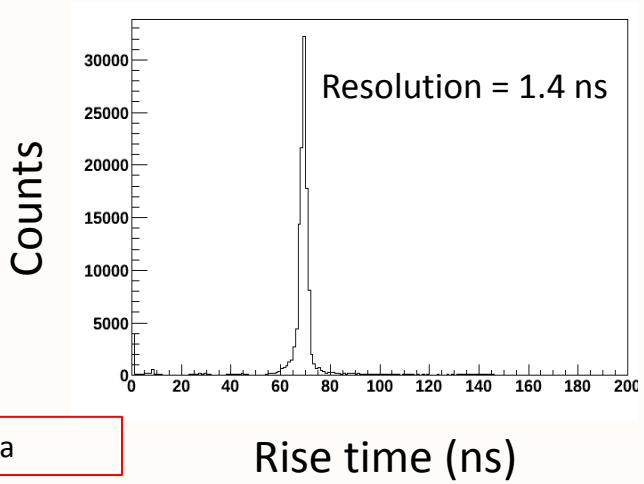


$^{7}Li + ^{89}Y$



Energy and Rise time Spectra ($^{7}Li + ^{197}Au$)

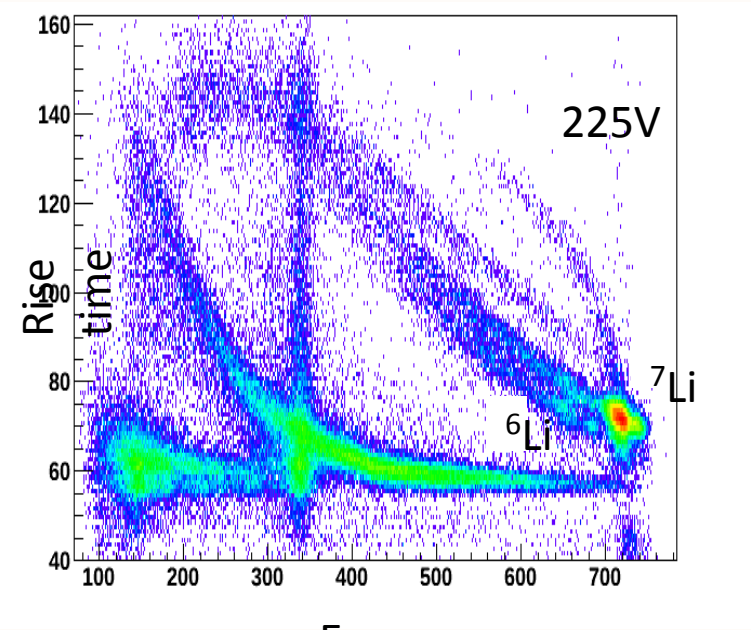




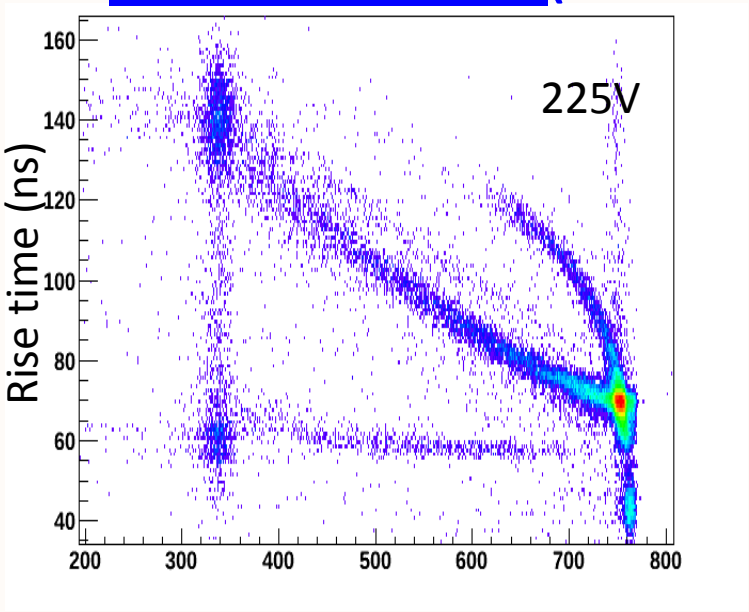
Ack:K. Mahata

Latest Results:

Energy vs Rise time: (^{7}Li +^{89}Y)



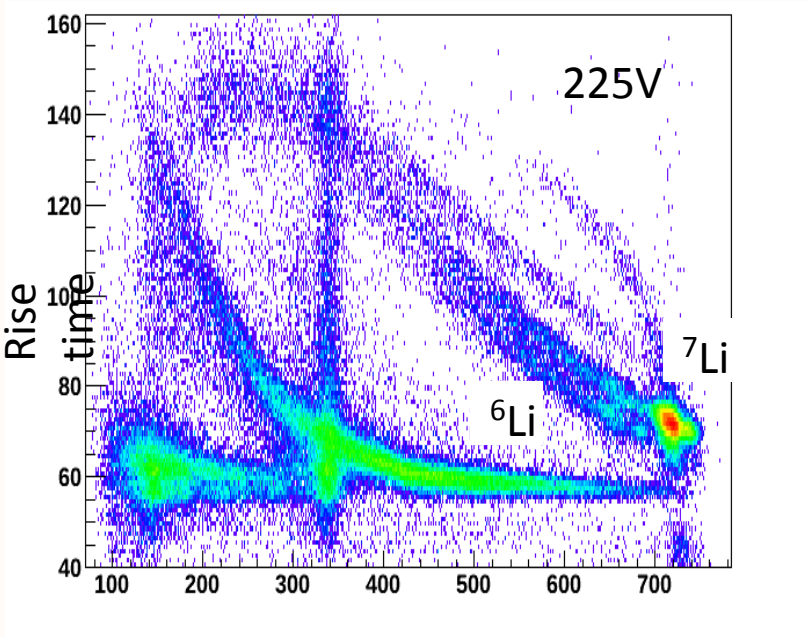
Energy vs Rise time (^{7}Li +^{197}Au)

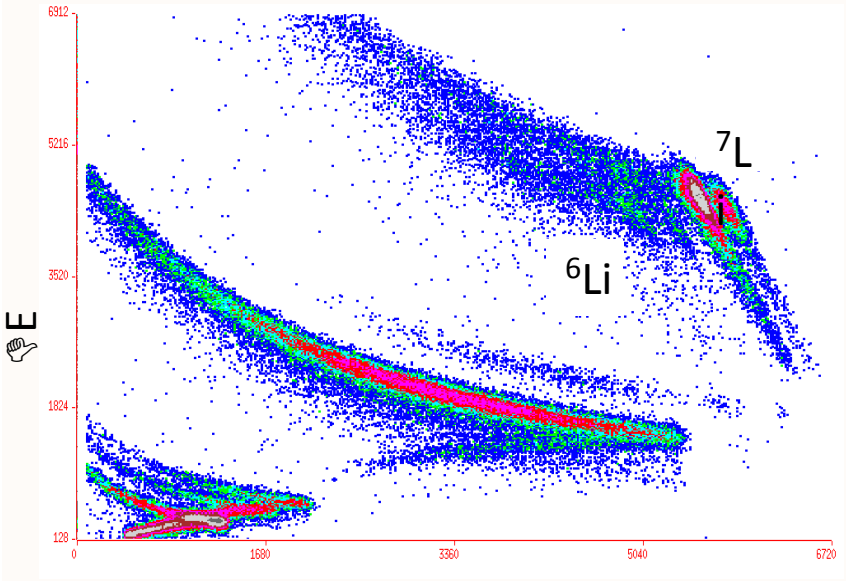


Ack:K. Mahata

Latest Results:

Energy vs Rise time and DE-E (mass separation)





Ack:K. Mahata

Conclusions:

- The card has been successfully used to implement two applications (viz LLRF controller and nuclear pulse acquisition).
- For both these applications data was successfully sampled at an effective sampling rate of 1Gsps.
- Individual components of the direct sampling LLRF controller have been successfully tested. Integration and testing of controller is in progress.
- The Am-Pu amplitude spectrum has a resolution of 75 KeV.
- Development of FPGA based filtering algorithms for nuclear pulse processing is on-going.
- Recently the card has been successfully used for pulse shape discrimination

THANK YOU