FAST DIGITAL FEED BACK CONTROL SYSTEMS FOR ACCELERATOR RF SYSTEM USING FPGA

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Abstract

Feedback control system plays important role for proper injection and acceleration of beam in particle accelerators by providing the required amplitude and phase stability of RF fields in accelerating structures. Advancement in the field of digital technology enables us to develop fast digital feedback control system for RF applications. Digital Low Level RF (LLRF) system offers the inherent advantages of Digital System like flexibility, adaptability, good repeatability and reduced long time drift errors compared to analog system.

To implement the feedback control algorithm, I/Q control scheme is used. By properly sampling the down converted IF signal using fast ADC we get accurate feedback signal and also eliminates the need of two separate detectors for amplitude and phase detection. Controller is implemented in Vertex-4 FPGA. Codes for control algorithms which controls the amplitude and phase in all four quadrants with good accuracy are written in the VHDL. I/Q modulator works as common actuator for both amplitude and phase correction. Synchronization between RF, LO and ADC clock is indispensable and has been achieved by deriving the clock and LO signal from RF signal itself. Control system has been successfully tested in lab with phase and amplitude stability better then ±1% and ±1° respectively. High frequency RF signal is down converted to IF using the super heterodyne technique. Super heterodyne principal not only brings the RF signal to the Low IF frequency at which it can be easily processed but also enables us to use the same hardware and software for other RF frequencies with some minor modification.

INTRODUCTION

A typical RF system of an accelerator consists of RF synthesizer, chain of amplifiers, RF cavity and other required sub systems. All these subsystems are realized using various active and passive components to fulfil the requirement for beam acceleration. Change in amplitude and phase characteristic of any of the component could lead to change in phase and amplitude of the EM field inside the cavity. To keep the amplitude and phase stable LLRF feedback control systems is used.

Block diagram of a typical Digital LLRF system is shown in the Fig. 1 which consists of four main components

- Synchronised LO and CLK generation
- RF to IF down conversion
- Digital controller
- Actuator

RF signal is first down converted to IF using mixer and appropriate LO signal. Synchronization between LO, RF and CLK is required for proper amplitude and phase detection. Controller is implemented in FPGA based digital signal processing board having fast ADC and DAC. The I/Q Modulator works as actuator to correct the amplitude and phase of RF signal. Digital signal processing schemes like CORDIC (COordinate Rotation DIgital Computer), PI (Proportional Integral) controller and digital filters are used to implement the proper algorithm. These schemes are implemented using Vertex-4 FPGA.

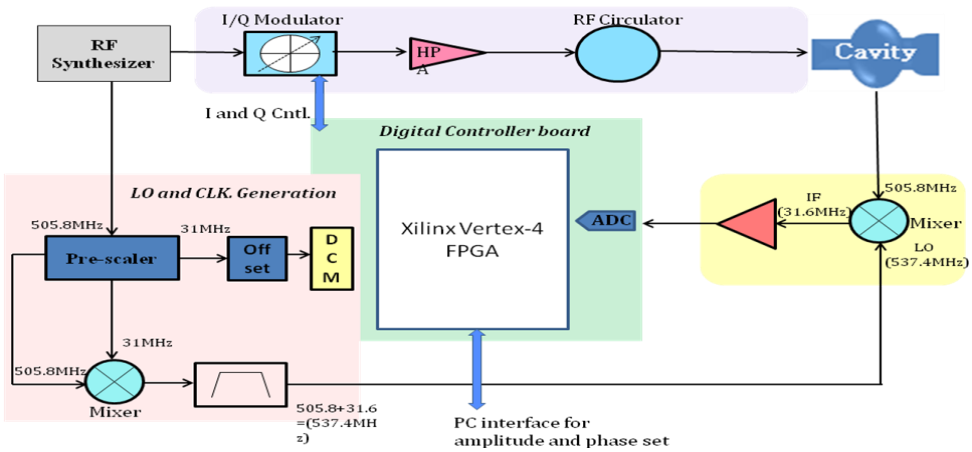

Figure 1: Block Diagram of Digital Feed Back Control System.

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SENSING AND DETECTION

Performance of the feedback control system strongly depends on the accuracy of the detection, hence proper sensing and detection of the amplitude and phase information of the RF signal is very important. As the processing of RF signal at very high frequency is difficult, super heterodyne scheme is used where the high frequency signal is down converted in to the Intermediate Frequency (IF) preserving the amplitude and phase information. This scheme allows us to use same system for different frequency with only minor modification.

Selection of IF frequency is done considering the maximum expected error rate and available hardware. We have chosen IF to be 31.6MHz for 505.8 MHz RF signal. Amplitude and phase information from the down converted IF signal is extracted using digital I/Q detection scheme. In Digital I/Q detection scheme two consecutive samples are taken 90° apart and separation of alternative samples gives us I and Q signal. This eliminates the need of two separate detectors for amplitude and phase detection. Selection of sampling frequency (f_s) is critical; which is governed by the relation shown in the Figure 2.

$$f_s = \frac{4}{4k+1} f_{RF} \text{ where } k = 0, 1, 2, \ldots$$

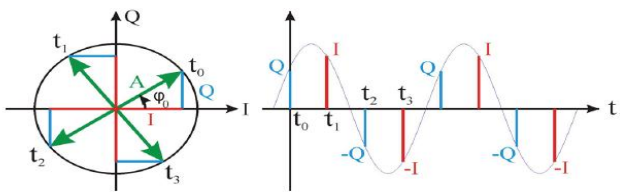

Figure 2: I/Q detection scheme.

Taking clock jitter, maximum error rate and available resources in consideration, a sampling frequency of ~25 MHz is selected.

SYNCHRONIZED LO AND CLOCK GENERATION

Synchronised RF, LO and clock signals were used to detect amplitude and phase of RF signal with good accuracy. To achieve this synchronization both LO and clock are derived from the main RF signal. LO (505.8+31.6 MHz) signal is required for Up/Down conversion of RF signal. Clock (25 MHz) signal is required for operation of ADC/ DAC. Using a pre-scalar 31.6 MHz (505.8/16) signal is produced which when mixed with 505.8 MHz RF signal gives the required LO signal. The same 31.6 MHz signal is used to generate the 25 MHz clock using DCM. This makes the LO and Clock both synchronised with RF signal. Performance of this scheme was tested by applying known phase shift to the RF signal and detecting this phase shift. Test results shown in Fig. 3 depict close resemblance between applied and detected phase shift.

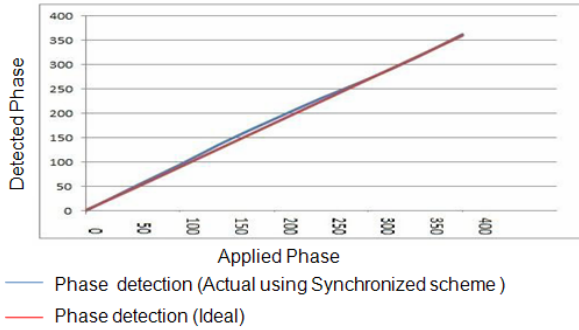

Figure 3: Phase detection characterization.

CONTROLLER

Purpose of the controller is to generate the control signal on the basis of set and detected signal. Controller is implemented in the vertex-4 FPGA board with 100 MSPs ADCs and DACs. Flow diagram of digital controller is shown in the Fig. 4

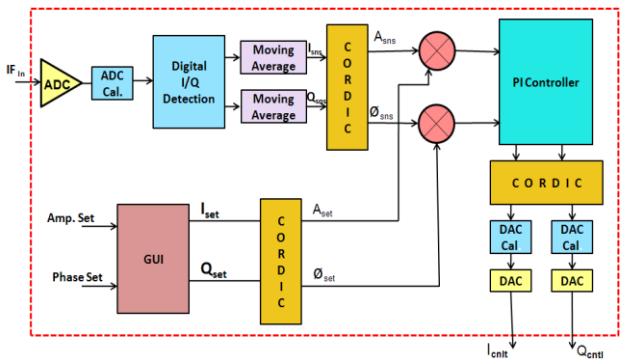

Figure 4: Controller flow chart.

Input IF signal is sampled by the ADC at a rate of ~25MHz to give the 'I' and 'Q' components of the IF signal. These sensed 'I' and 'Q' components of the IF signal are compared with the set 'I' and 'Q' components. Control algorithm is written in VHDL to generate the required I and Q control signal. Single ended to differential converter is also implemented to make I/Q control signal compatible to I/Q modulator. These differential 'I' and 'Q' control signals are fed to I/Q modulator to generate the corrected RF output signal. To rotate the control signal in the circle for producing correction CORDIC algorithm is used. Movement of the control vectors are shown in the Fig. 5

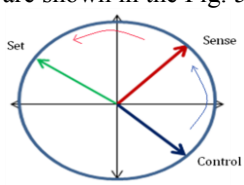

Figure 5: Rotation of vectors for control system.

I/Q MODULATOR

In order to correct the amplitude and phase error actuator is needed, which should be able to change the

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amplitude and phase as per the control signal. I/Q modulator is used to control the amplitude and phase.

$$RF_{out}(t) = I.A_{RF}\sin(\omega t) + Q.A_{RF}\cos(\omega t) = A_{out}\sin(\omega t + \phi)$$

$$A_{out} = A_{RF}\sqrt{I^2 + Q^2} \quad and \quad \phi = \tan^{-1}\left(\frac{Q}{I}\right)$$

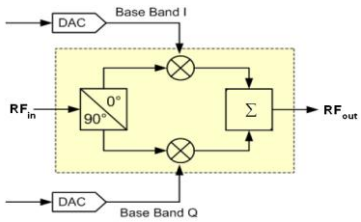

Figure 6: Typical Block diagram of I/Q modulator.

As depicted in Fig. 6 change in base band I and Q signal will change the amplitude and phase of the RF signal allowing the control of amplitude and phase of the RF signal. These base band I/Q signals are generated by the controller to correct the error in the signal.

TEST SET UP AND RESULTS

For testing of the digital LLRF control system test bench was set up in the lab. The block diagram of test setup is shown in Fig. 7.

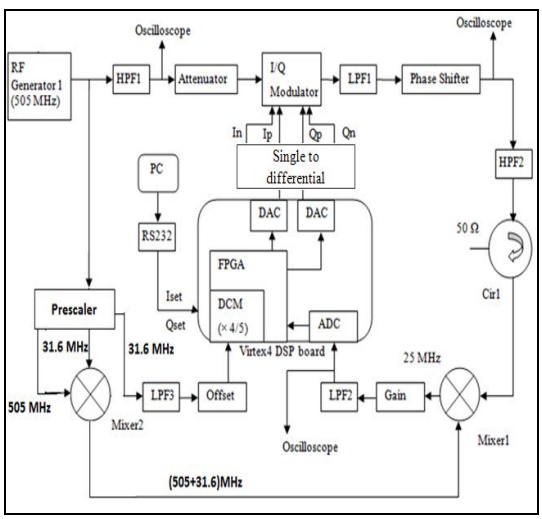

Figure 7: Block diagram of the test setup.

Amplitude and phase errors are deliberately introduced and performance of the system is checked under closed loop and open loop condition. Amplitude correction for the 20dB dynamic range and phase correction of the full 360 degree has been successfully achieved. Results along with the photograph of actual test bench are shown in the Fig. 8.

Test on the amplitude and phase stability of the system was also performed. Amplitude stability of better than 0.5% and phase stability better than 0.5º has been achieved. Results are shown in Fig. 9.

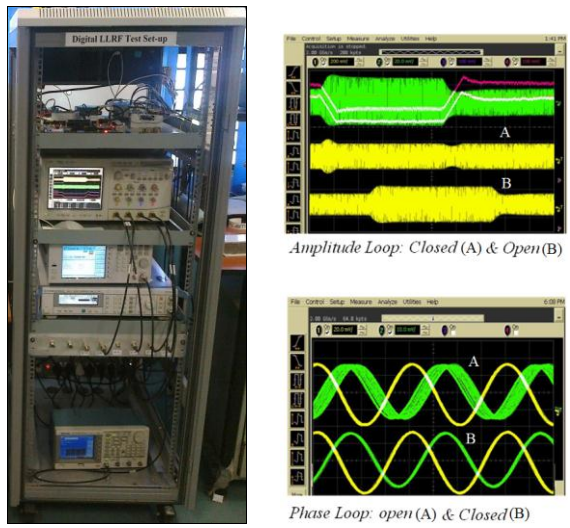

Figure 8: Photograph of test bench and test results.

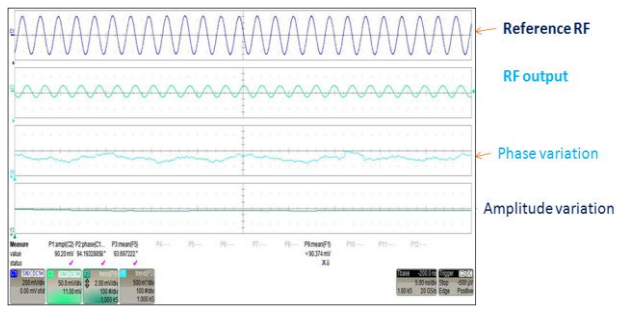

Figure 9: Amplitude and Phase Stability Results.

CONCLUSION

Digital Low Level RF control system has been developed. Testing of the closed loop system has been successfully done in the lab. This Digital LLRF system will be implemented in Indus-2 RF system which is being upgraded. With slight modification same system can be used for machine at different frequency. Use of digital processor like FPGA will also allow us to incorporate different diagnostic for RF system in future.

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