

COTS Technology for High Energy Physics Instrumentation

Kevin Schultz
Vice President, R&D
National Instruments





“I invented nothing new. I simply assembled into a car the discoveries of other men behind whom were centuries of work. . . .

Had I worked fifty or ten or even five years before, I would have failed. So it is with every new thing.”

— Henry Ford

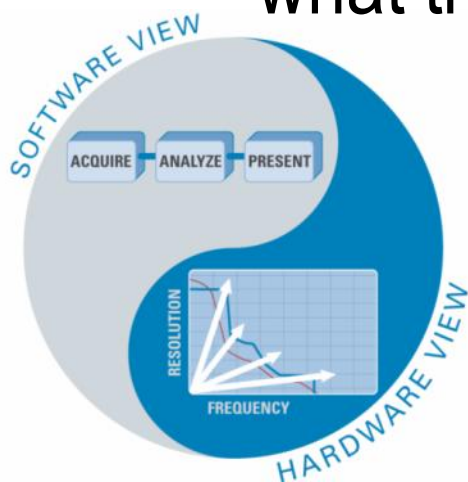
Innovation often means moving existing ideas
from where they're known to where they're not—
often in new combinations.

bridging distant worlds
and
building new worlds

*“... to do for scientists and engineers,
what the spreadsheet did for financial
analysts ...”*

The National Instruments Vision

“To do for scientists and engineers
what the spreadsheet did for financial analysis.”

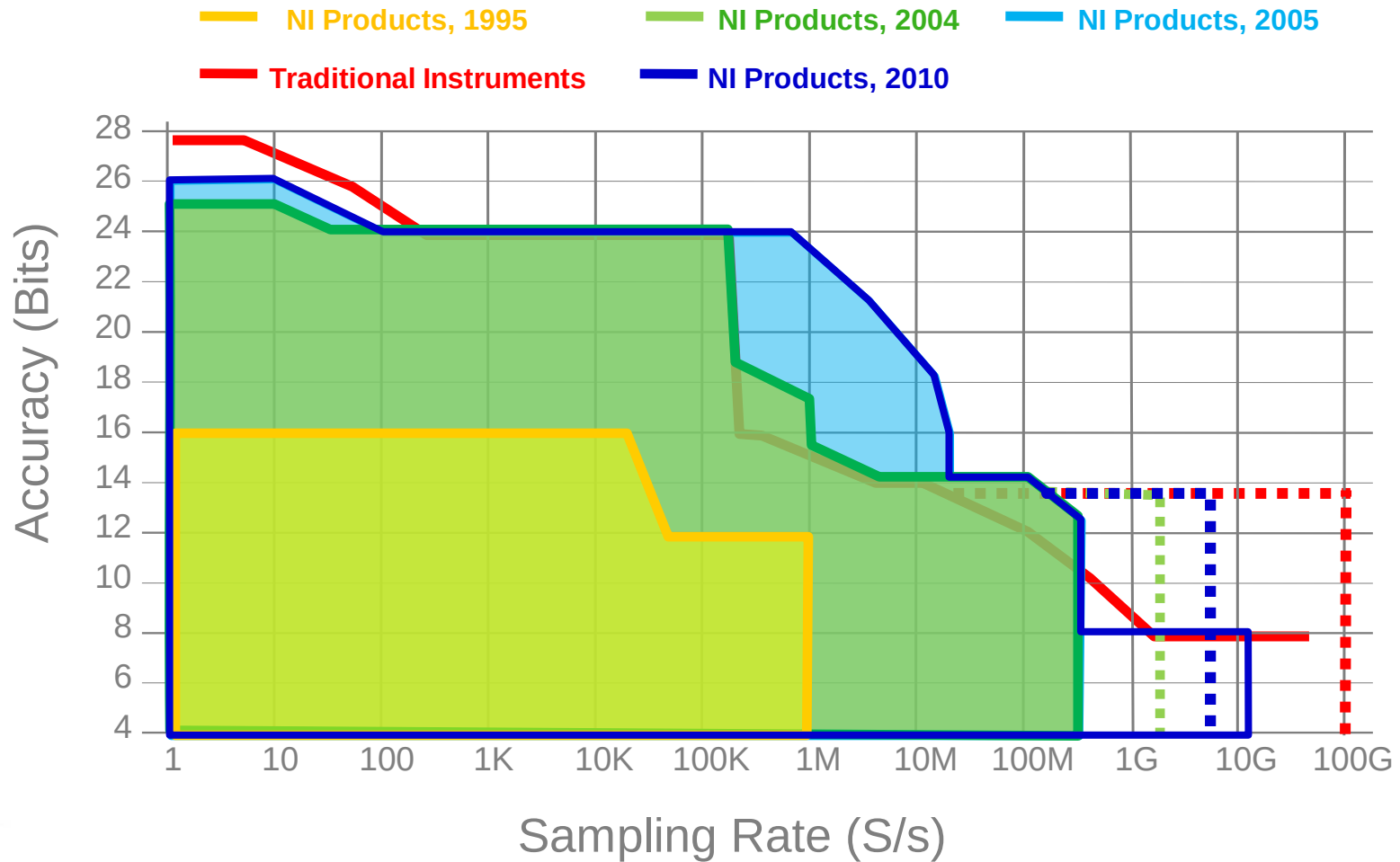


Virtual Instrumentation



with **NI LabVIEW™**

Leveraging Semiconductor Technology



POWERED BY

NATIONAL INSTRUMENTS

LabVIEW™



Diversity of Applications

No Industry > 10% of Revenue



Telecom



Automotive



Semiconductors



Electronics



Computers



ATE



Military/Aerospace



Advanced
Research &
Big Physics



Petrochemical

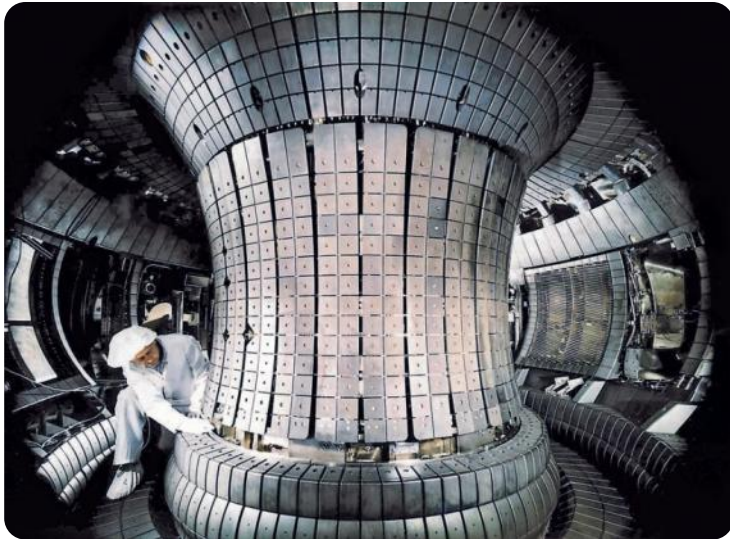


Food
Processing

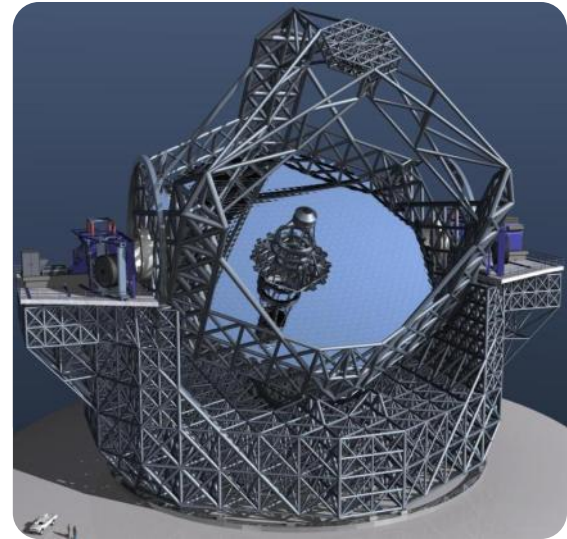


Textiles

Today's Control System Challenges



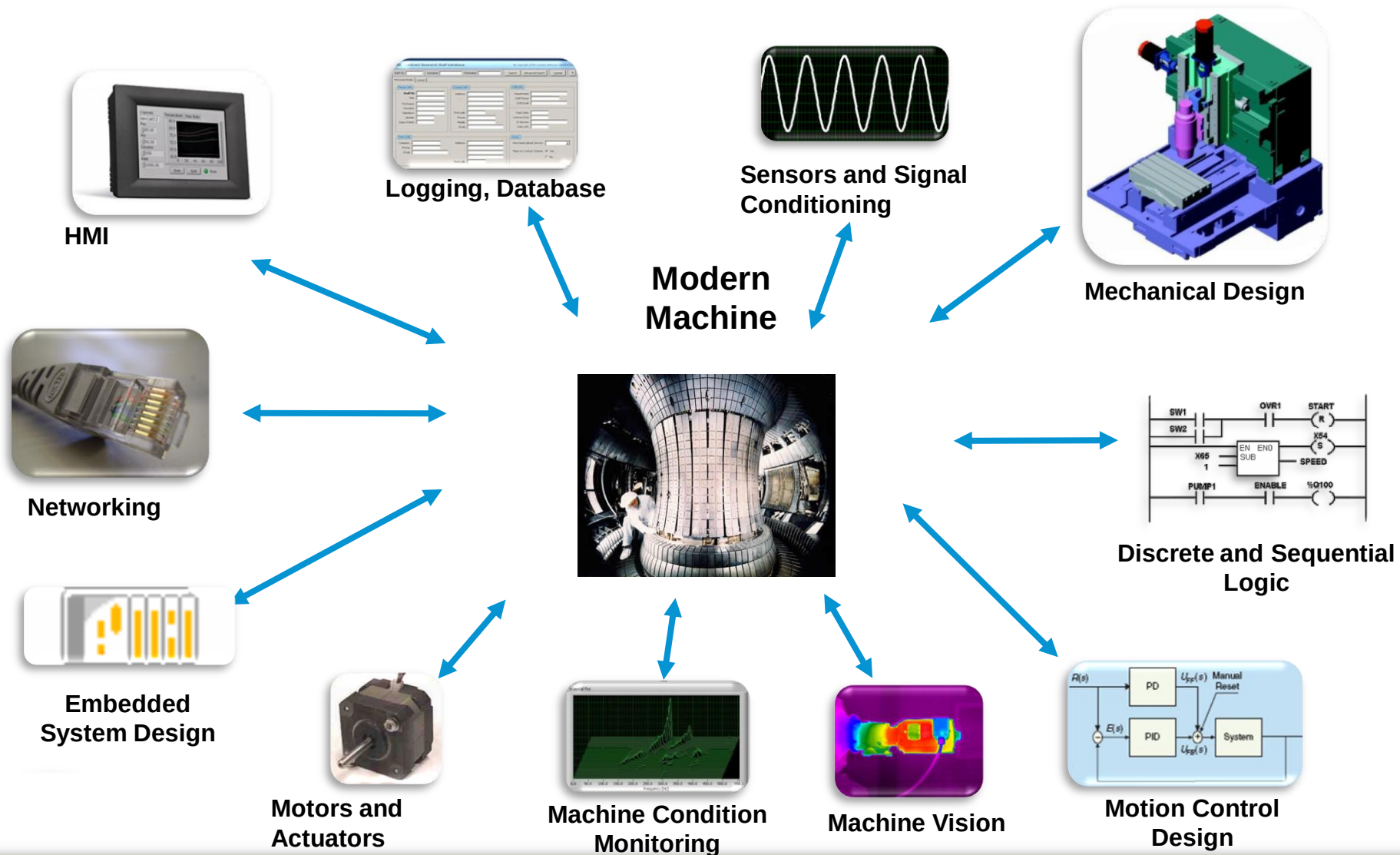
**ITER - Plasma
Diagnostics & Control**



**ESO Extremely Large
Telescope - Mirror Control**

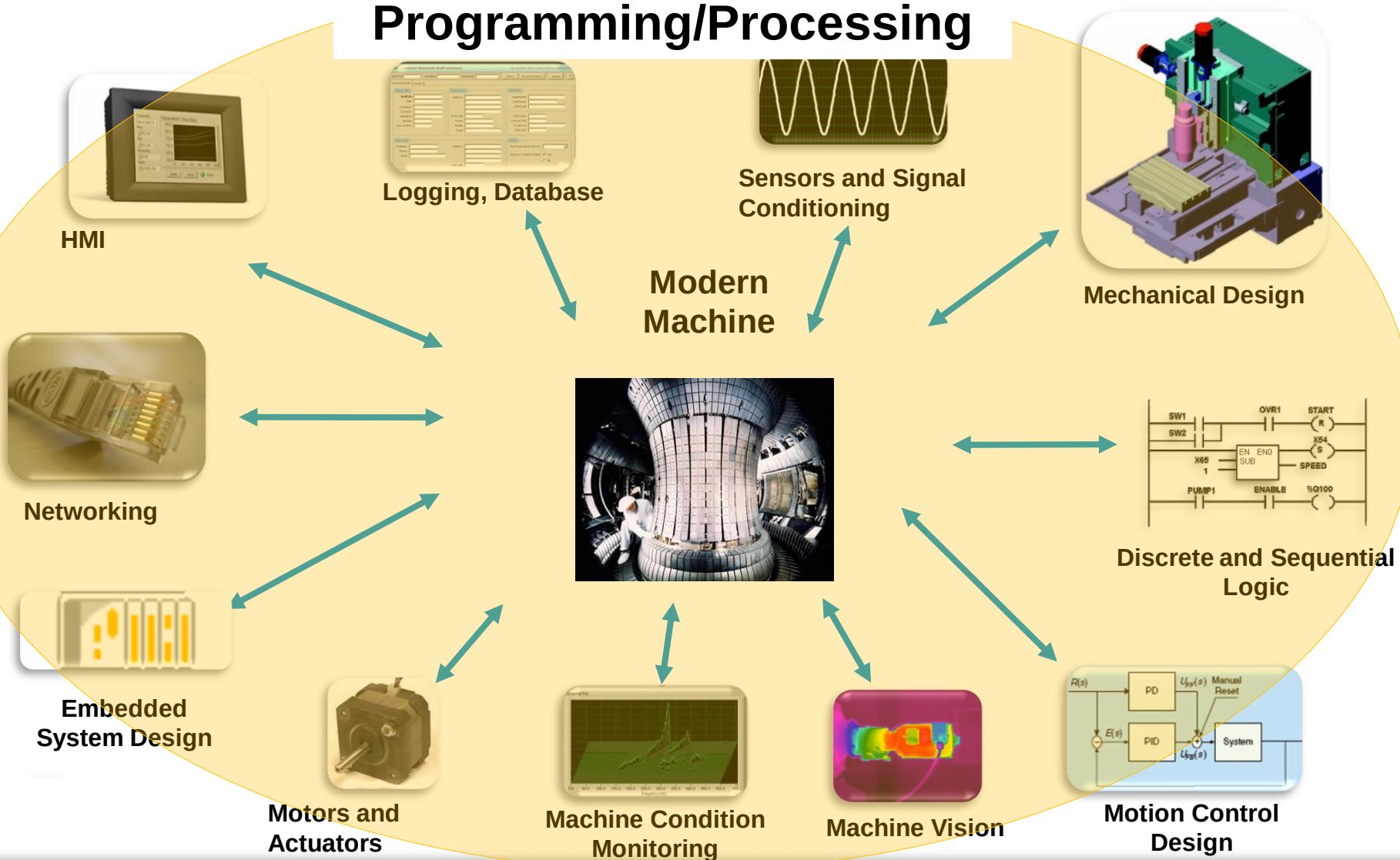
Modern system complexity is increasing

Modern System Complexity Increasing



Modern System Complexity Increasing

Programming/Processing



Modern System Complexity Increasing

Programming/Processing

Communication

Modern Machine



HMI

Logging, Database

Sensors and Signal Conditioning

Mechanical Design

Networking

Discrete and Sequential Logic

Embedded System Design

Motors and Actuators

Machine Condition Monitoring

Machine Vision

Motion Control Design

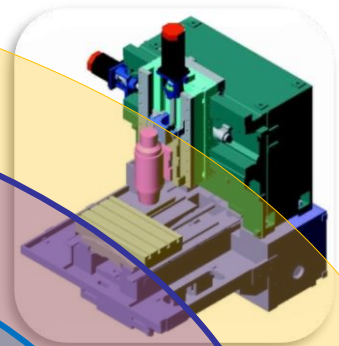
Modern System Complexity Increasing

Programming/Processing

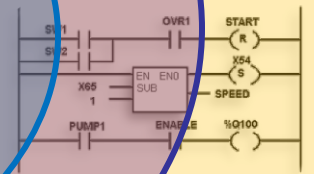
Communication

Timing/Sync

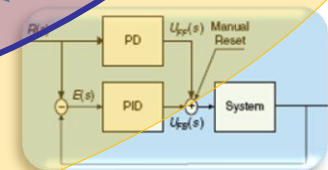
Modern Machine



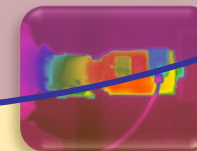
Mechanical Design



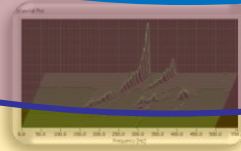
Discrete and Sequential Logic



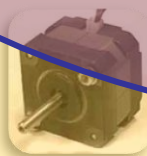
Motion Control Design



Machine Vision



Machine Condition Monitoring



Motors and Actuators



Embedded System Design



Networking



HMI



Logging, Data

Sensors and Signal

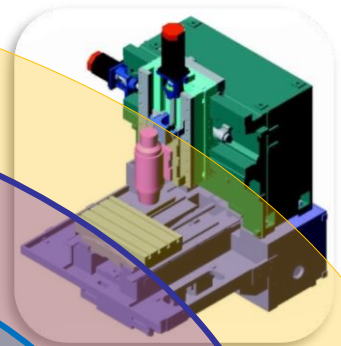
Modern System Complexity Increasing

Programming/Processing

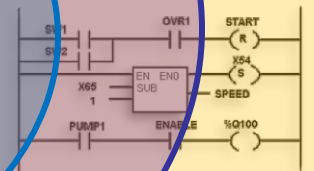
Communication

Timing/Sync

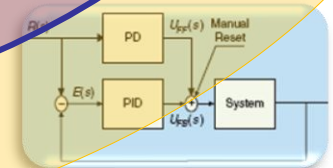
Custom HW



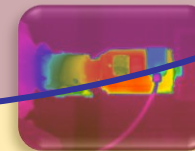
Mechanical Design



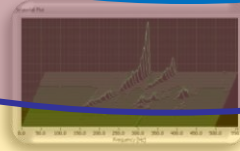
Discrete and Sequential Logic



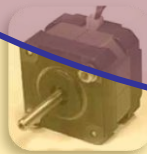
Motion Control Design



Machine Vision



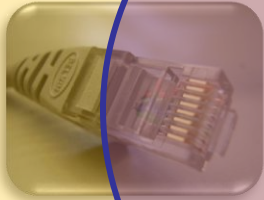
Machine Condition Monitoring



Motors and Actuators



Embedded System Design



Networking



HMI

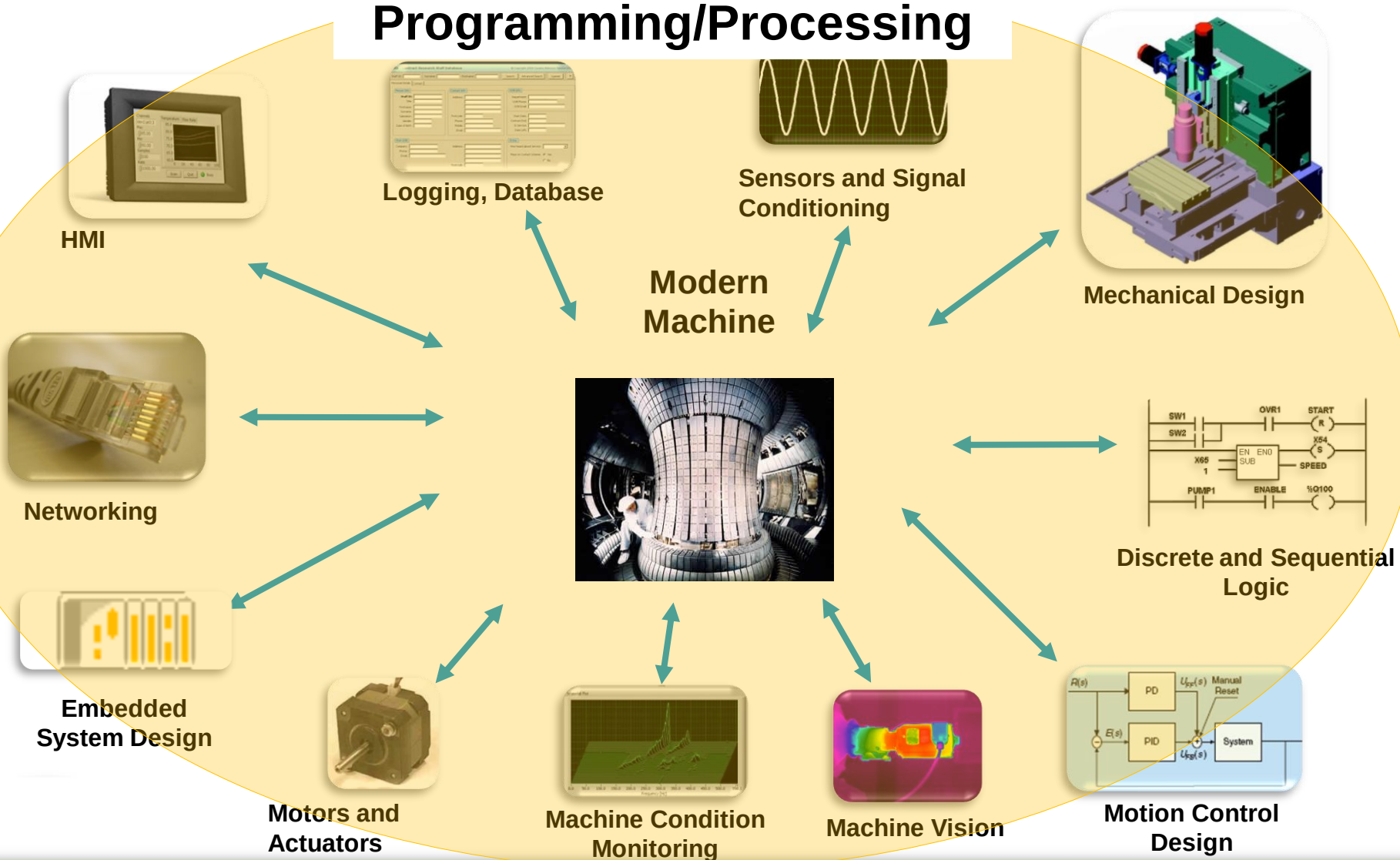


Logging, Data

Sensors and Signal

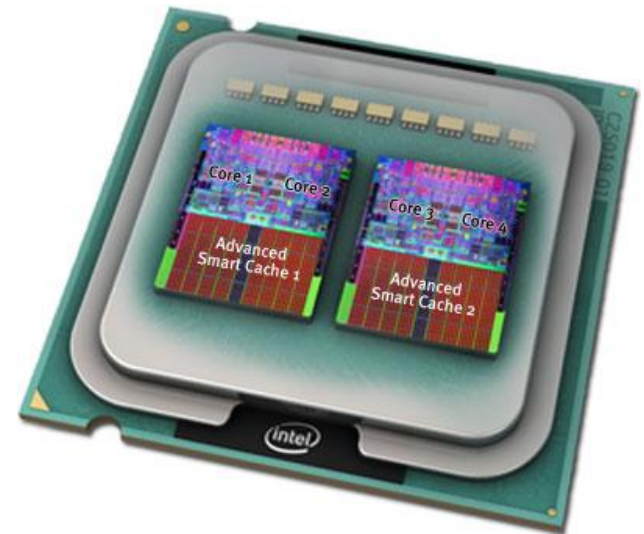
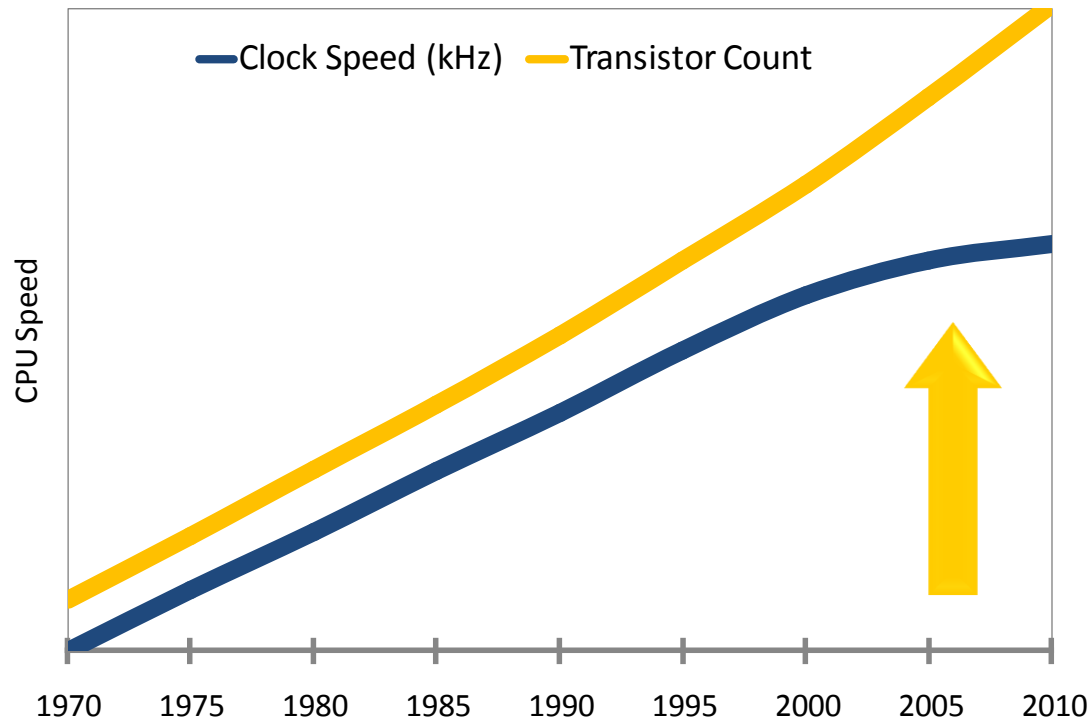
Modern System Complexity Increasing

Programming/Processing



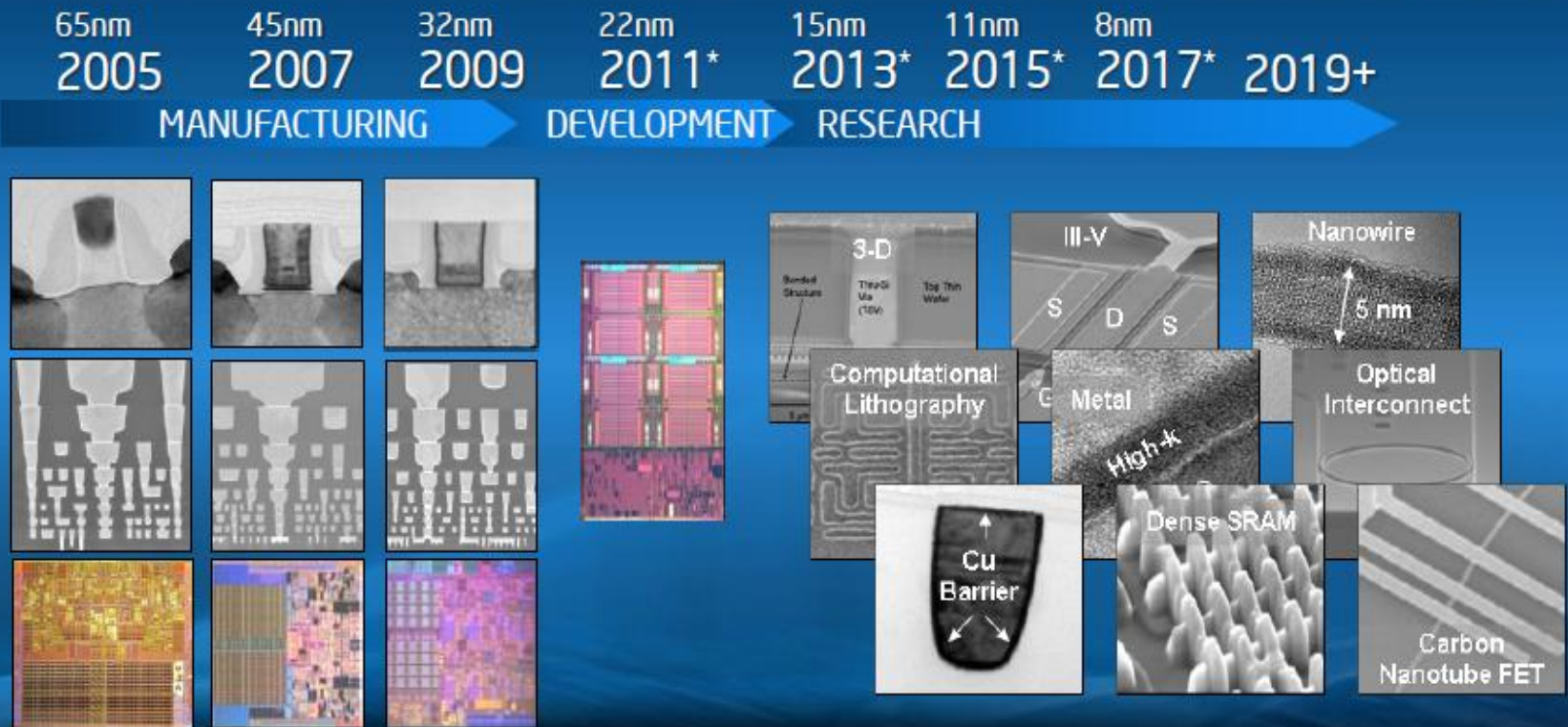
Moore's Law

Driving the computer revolution over the last 20 years



Multicore Processors

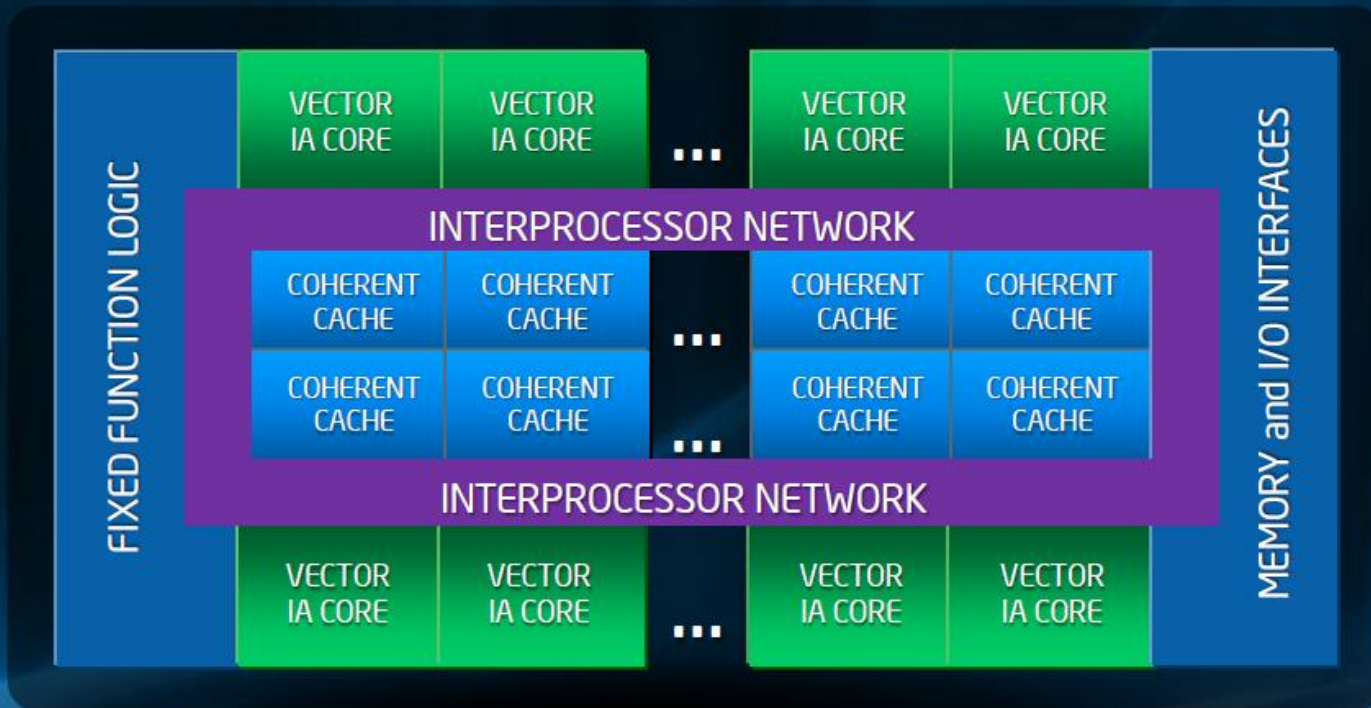
Moore's Law: Alive and Well at Intel



Intel Innovation-Enabled Technology Pipeline is Full



Intel® MIC Architecture: *An Intel Co-Processor Architecture*



Many cores and many, many more threads
Standard IA programming and memory model

Traditional Development Tool Mine Field

Priority Inversion

Deadlock/Livelock

Thread Synchronization

Processor Cache Effects

Race Conditions

Scalability to Multiple CPUs

Sequential Performance

Lock Contention

Flow of Data

Non-Determinism

Load Balancing

The Parallel Programming Challenge



Microsoft®

“The concurrency revolution is likely to be more disruptive than the OO revolution...”

- Herb Sutter, CEO, Microsoft, The Free Lunch is Over



"Parallel programming is perhaps the largest problem in computer science today"

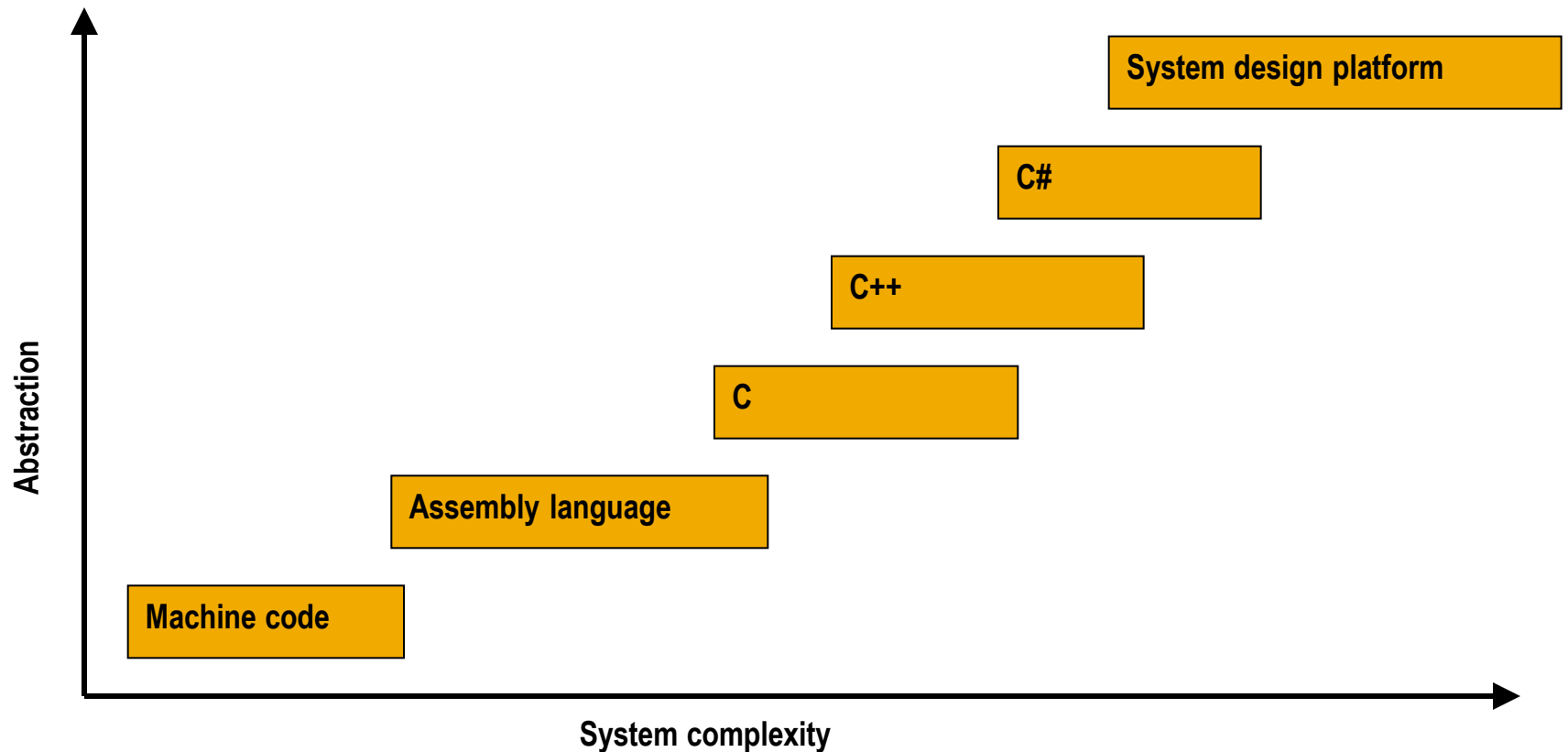
- Stanford CS Department chair Bill Dally



“Nobody knows how to program those things”

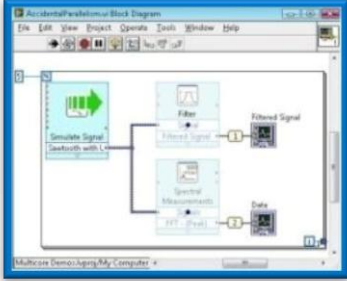
— Steve Jobs talking about multicore processors

Increasing Levels of Software Abstraction



High-Level Design Models

Data Flow



C Code

[illegible]

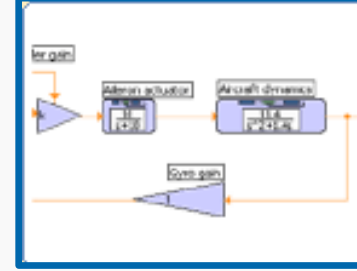
Textual Math

```

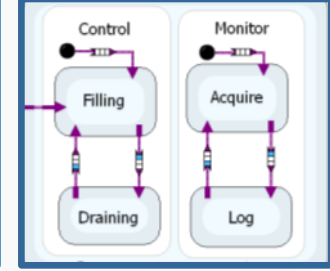
1  A = [1 3; 4 2];
2  B = [6 7; 2 3];
3  C = A*B;
4  eigC = eig(C);
5  D = k*A

```

Simulation



Statechart



NATIONAL INSTRUMENTS



Graphical System Design Platform



PC/Mac/Linux



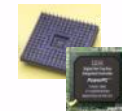
PXI



CompactRIO

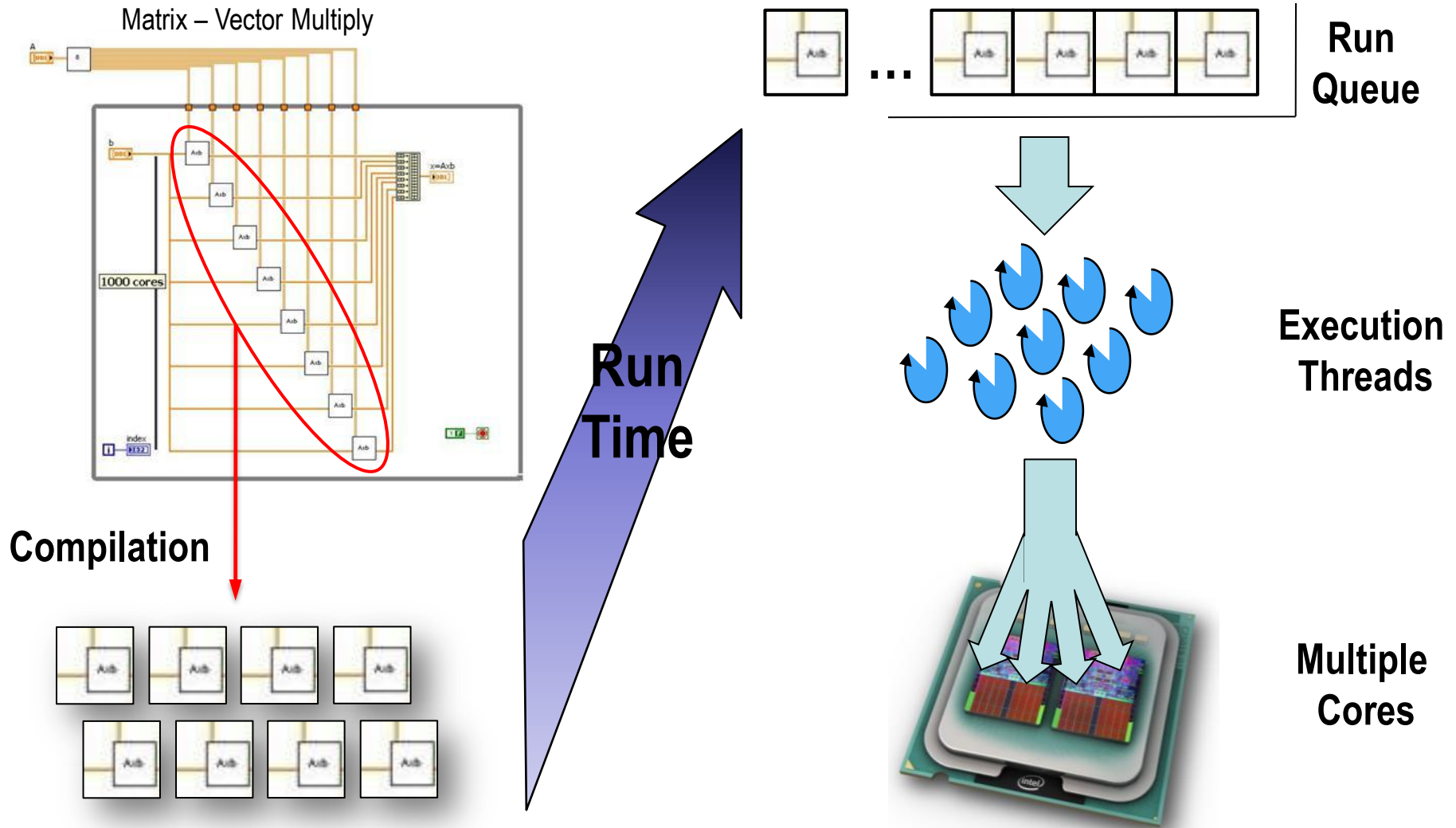


FlexRIO



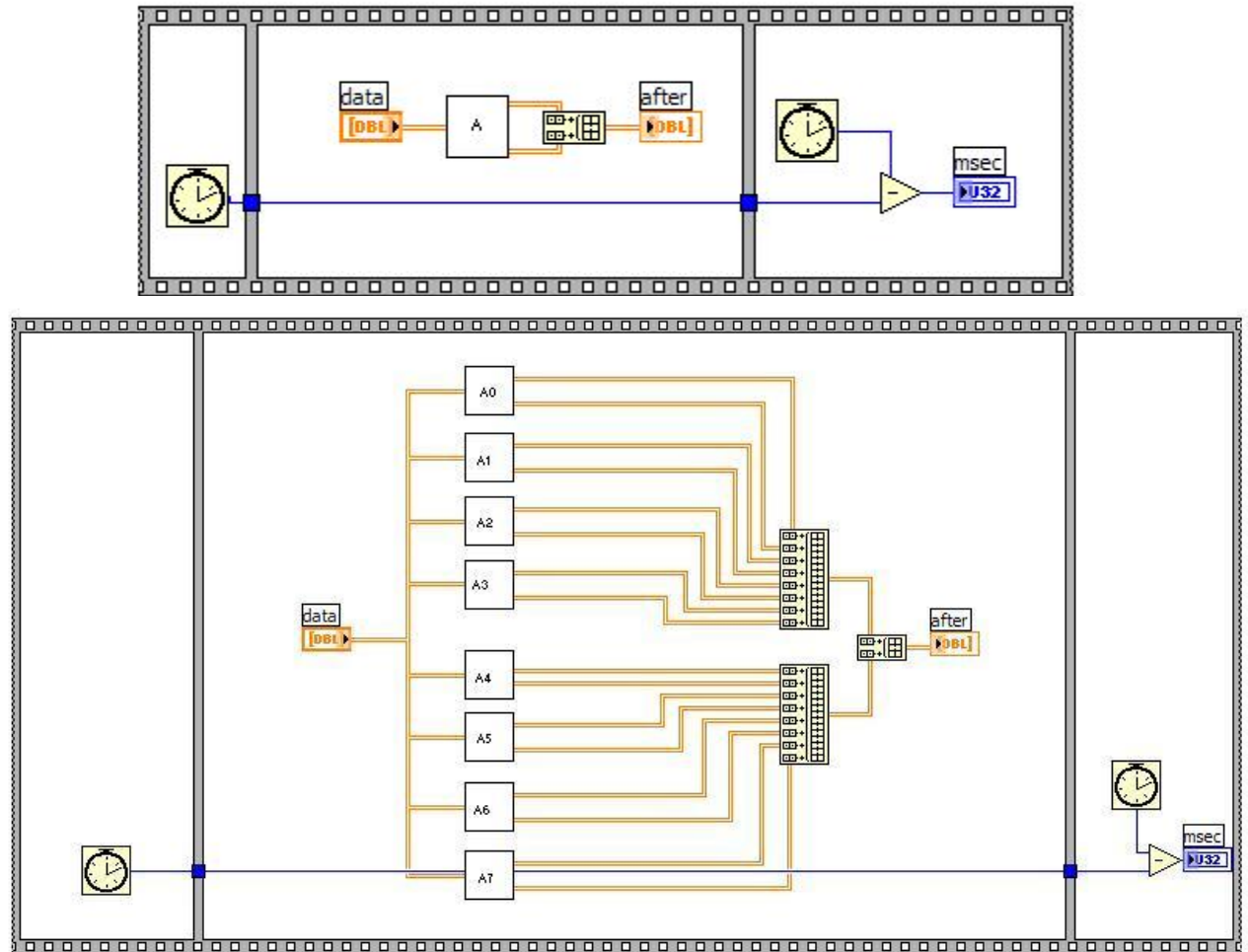
Custom

LabVIEW Execution Fundamentals

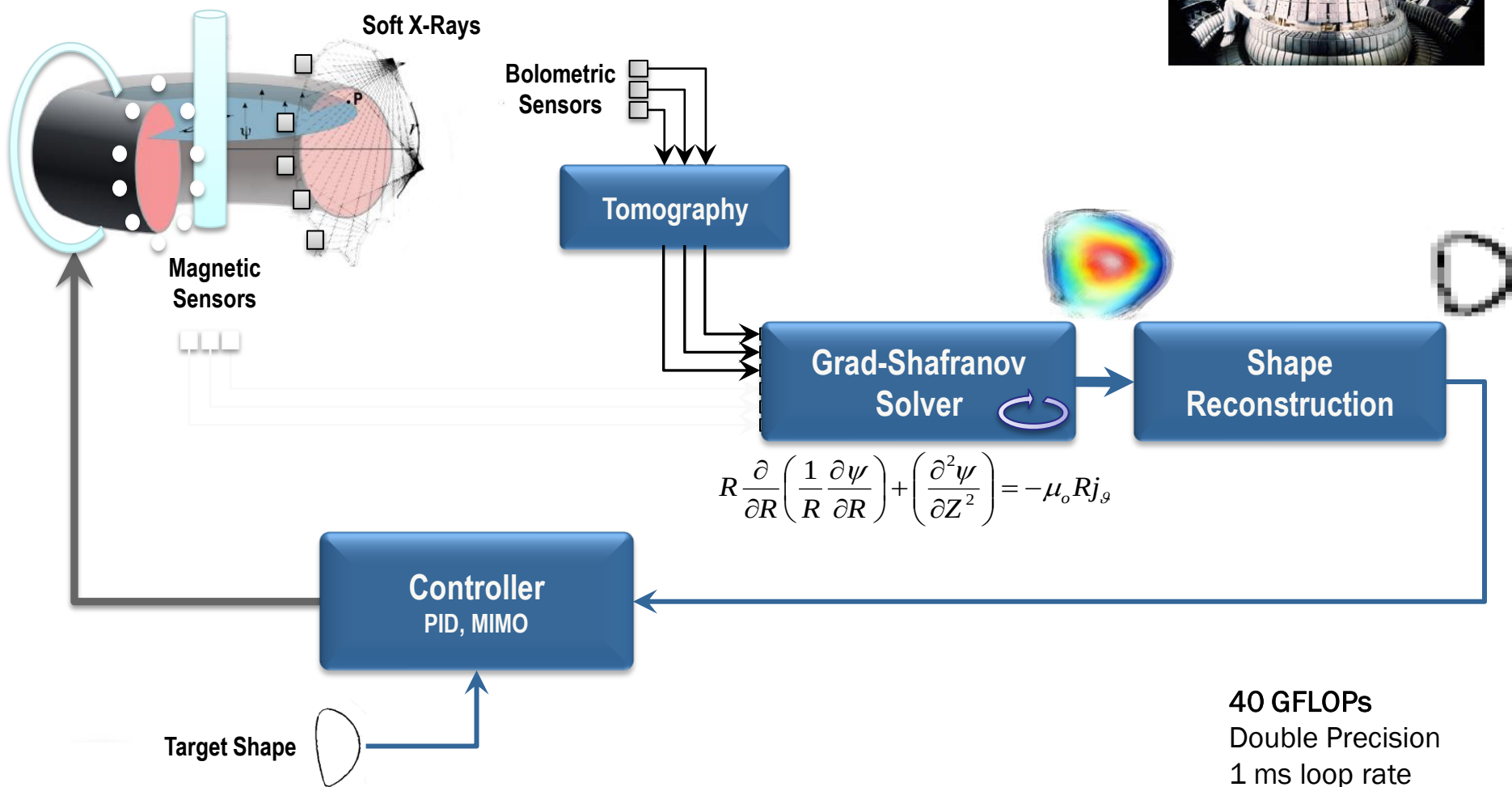


From 1 to 8 cores

cores	time [ms]
1	4.2
2	2.3
4	1.2
8	0.6



Tokamak – Shape Control



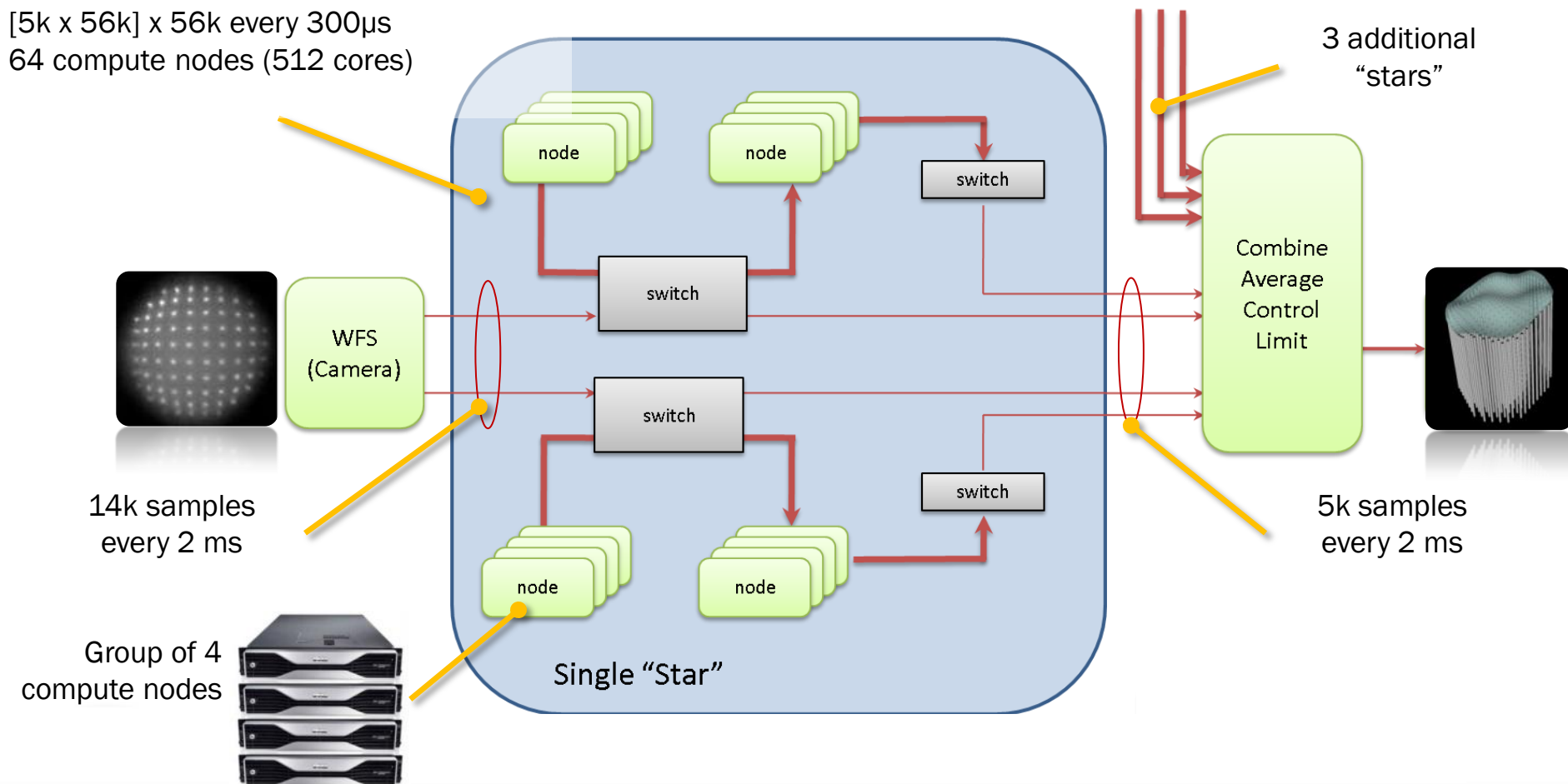
Extremely Large Telescope Design

ESO-E Mirror 4 (M4) Wavefront Real-Time Computing

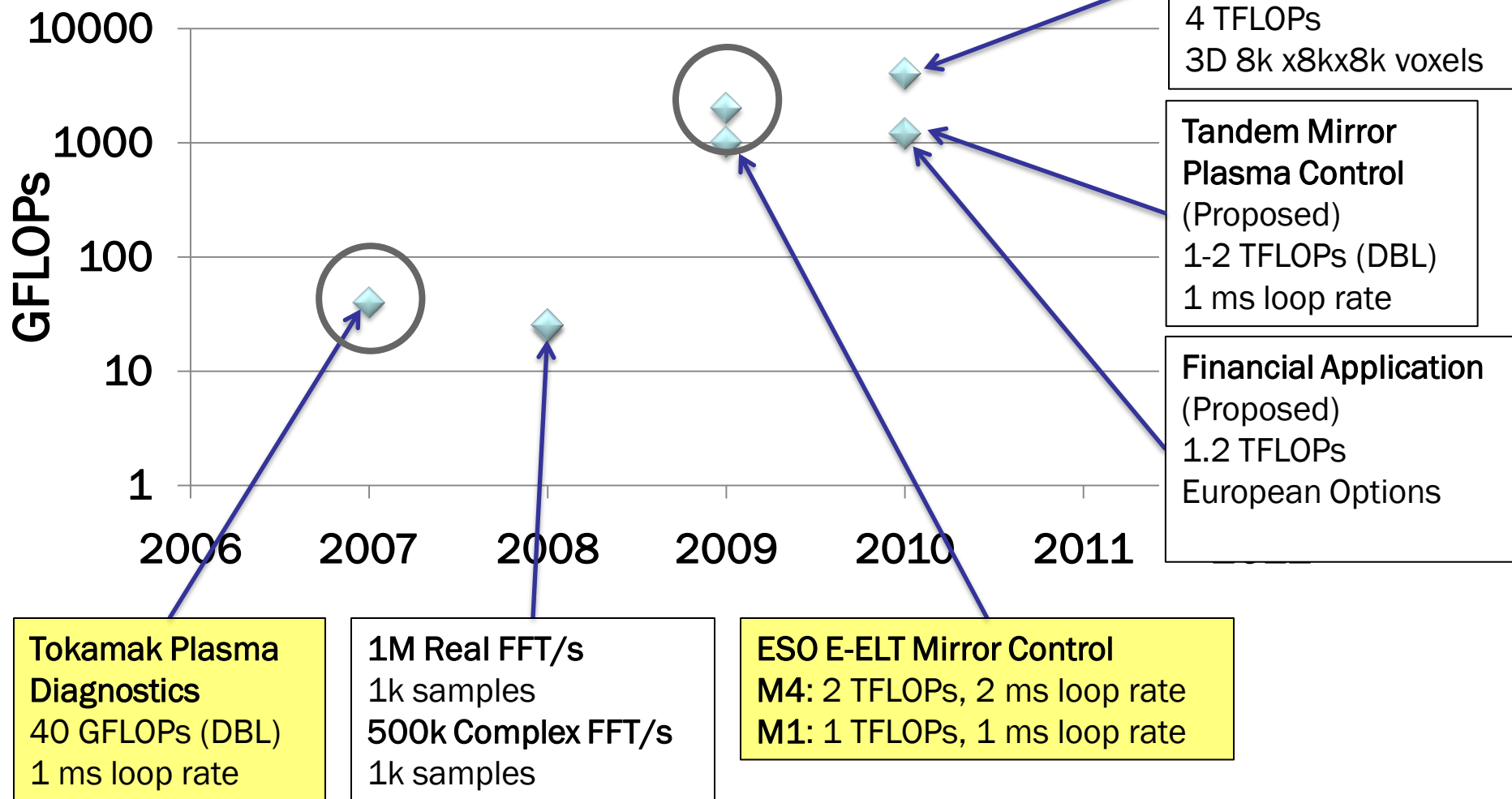
1.87 TFLOPs

[5k x 56k] x 56k every 300 μ s

64 compute nodes (512 cores)



Real-Time HPC Trend

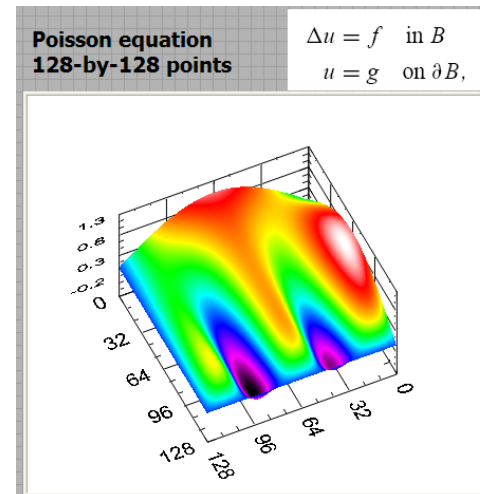


Plasma Diagnostics & Control with NI LabVIEW RT



Max-Planck-Institut
für Plasmaphysik

- Poisson PDE
 - Fourier/DST
 - Hockney
 - Cyclic reduction
 - Combination method
- **N-cores require specific parallelization strategies**
- **Goal: 1 ms sustained and in a highly deterministic way**



Plasma Diagnostics & Control with NI LabVIEW RT



Max-Planck-Institut
für Plasmaphysik

- Plasma control in nuclear fusion Tokamak with LabVIEW on an eight-core real-time system
- “...with LabVIEW, we obtained a **20X processing speed-up** on an octal-core processor machine over a single-core processor...”*

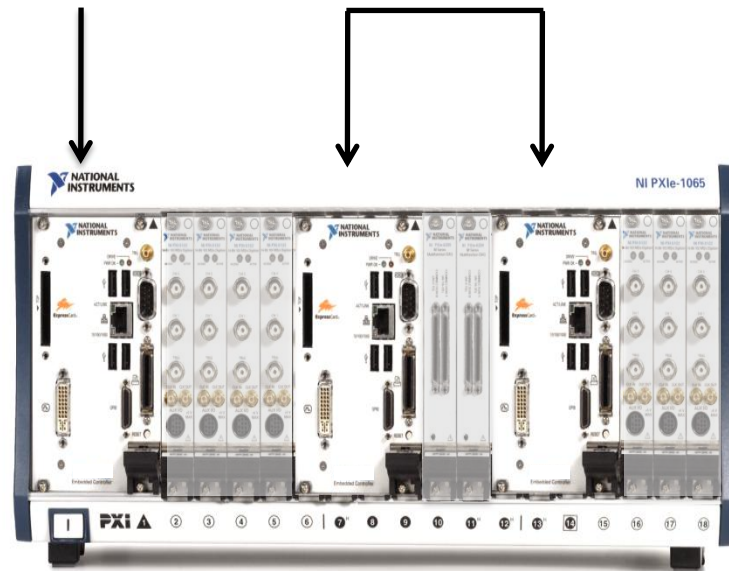
Louis Giannone
Lead Project Researcher
Max Planck Institute



PXI Multi-Chassis (PXImc)

System
Controller

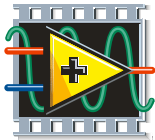
PXImc Processor
Modules



One Way Latency = 6 μ S, Throughput = 670 MB/S

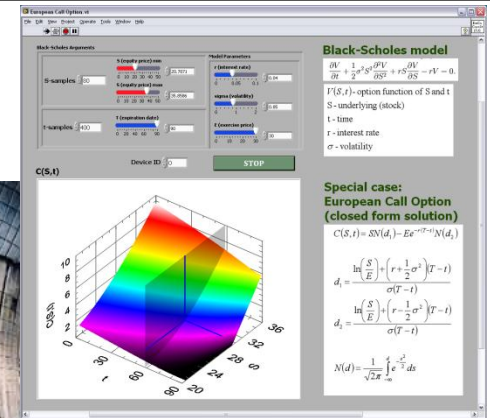
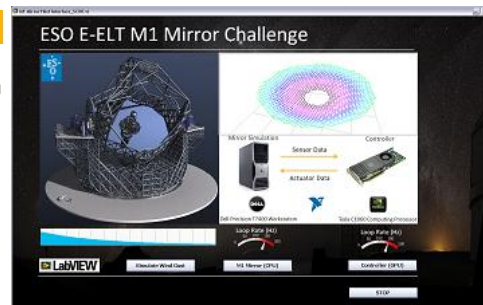
LabVIEW's GPU Computing Module

POWERED BY



NATIONAL INSTRUMENTS

LabVIEW™



C
C++

OpenCL™

DirectX
Compute

FORTRAN

Java and
Python



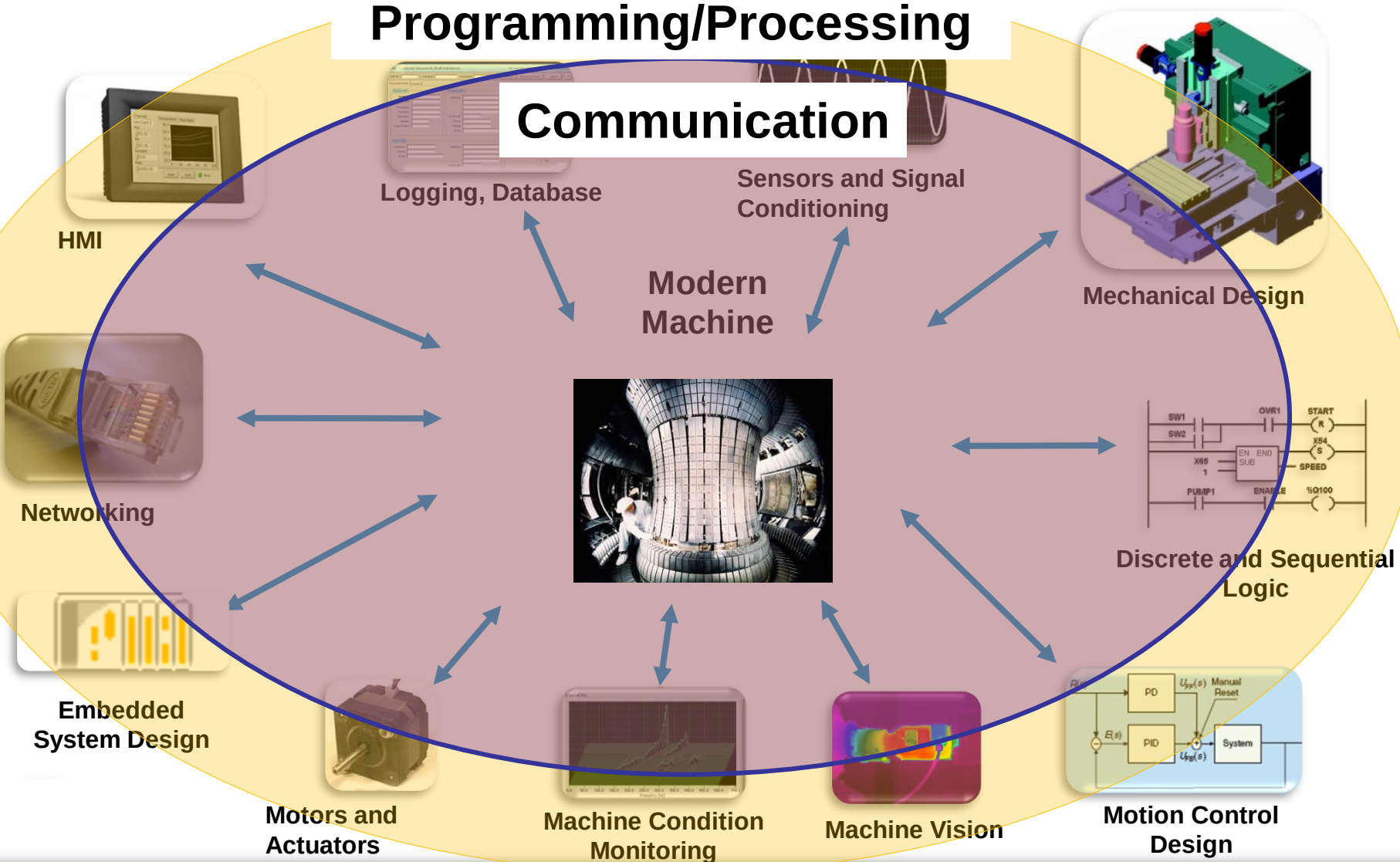
NVIDIA GPU

with the CUDA Parallel Computing Architecture

Modern System Complexity Increasing

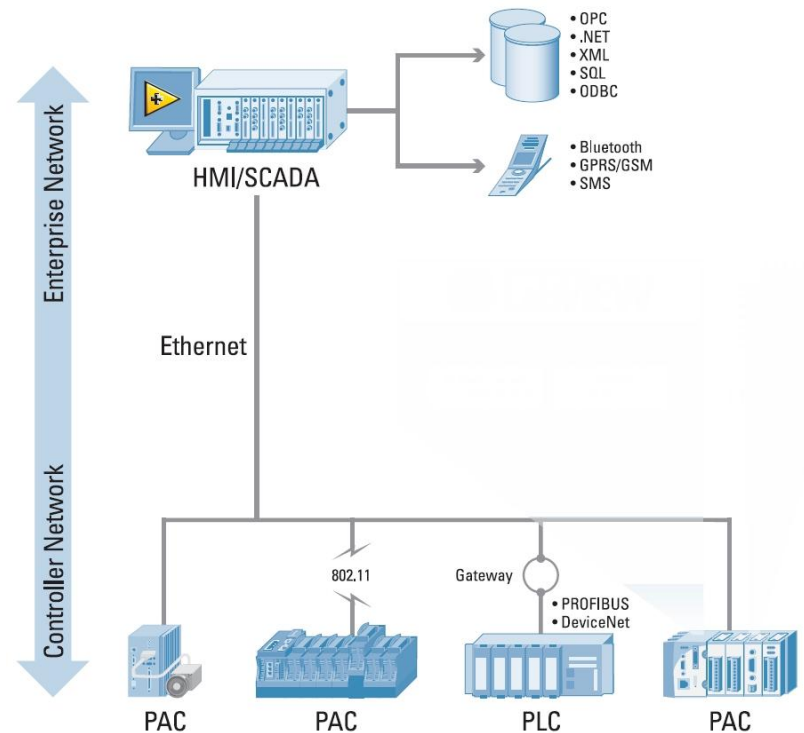
Programming/Processing

Communication

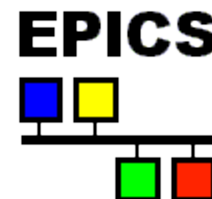


Open Architecture

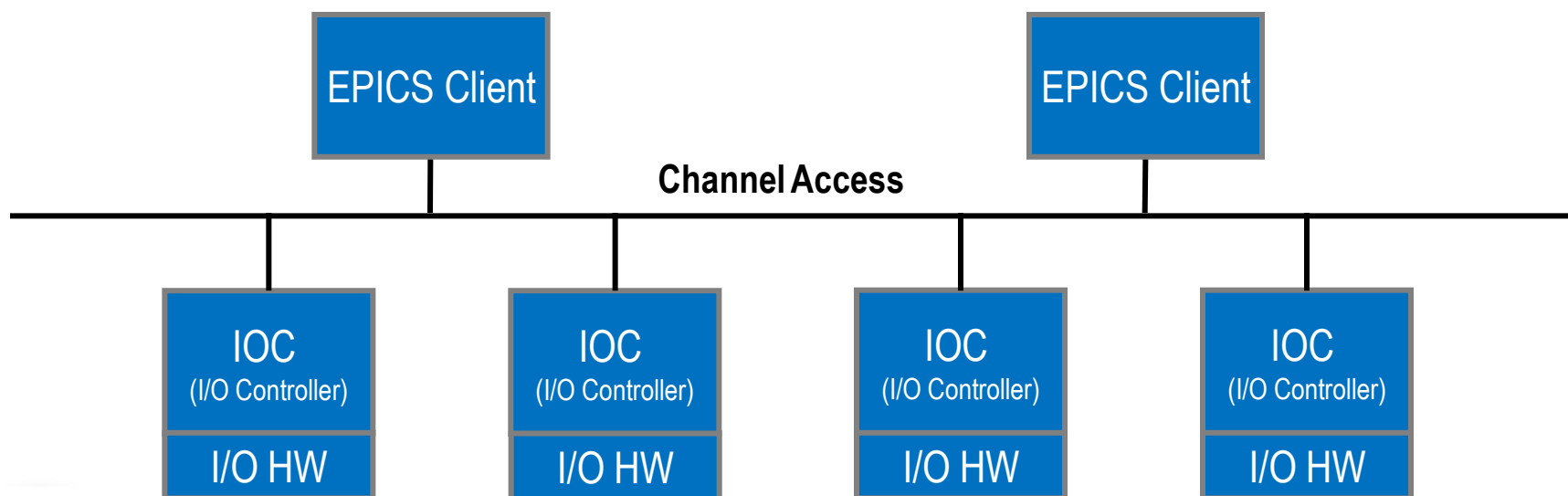
- Controls standards
 - EPICS, TANGO, CORBA, TINE, C
- Connectivity to different devices
 - OPC, Modbus, TCP/IP, UDP, EtherCAT, Serial
- Flexibility
 - Windows, RTOS, Linux, FPGA



EPICS Software Architecture



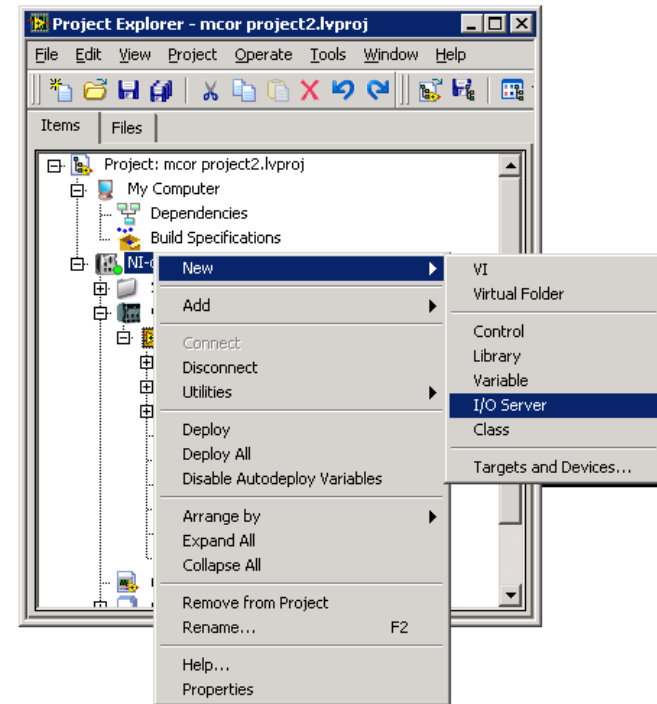
- Distributed Clients and Servers (IOC – I/O Controllers)
- Network protocol: Channel Access
- Each IOC holds a subset of EPICS database variables



Analog I/O, Digital I/O, Motion Control, Image Acquisition, etc.

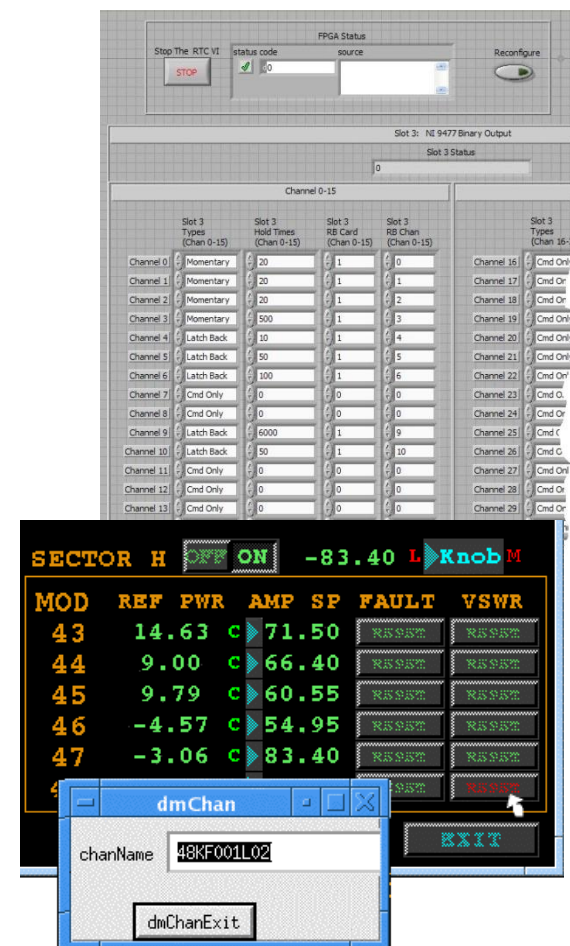
EPICS in LabVIEW

- Support for Channel Access server and client
 - Windows
 - RT – VxWorks & Pharlap (Server only)
- Prototype code to run full EPICS IOC Server side by side with LabVIEW Real-Time
 - Custom option for CompactRIO



Los Alamos LANSCE

- Ongoing migration to a cRIO system with embedded EPICS
 - 12 binary outputs
 - 36 binary inputs
 - 12 analog inputs
 - 5 stepper motor channels
- Full IOC functionality allows access to all record fields and EPICS utilities
- Maximum flexibility for partitioning the problem
 - LabVIEW for beam diagnostic
 - EPICS for industrial control



Modern System Complexity Increasing

Programming/Processing

Communication

Timing/Sync

Modern Machine



HMI

Logging, Data

Sensors and Signal

Mechanical Design

Networking

Discrete and Sequential Logic

Embedded System Design

Motors and Actuators

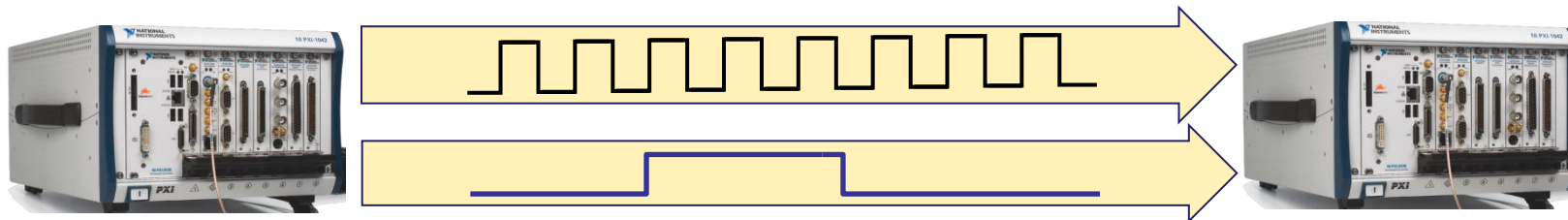
Machine Condition Monitoring

Machine Vision

Motion Control Design

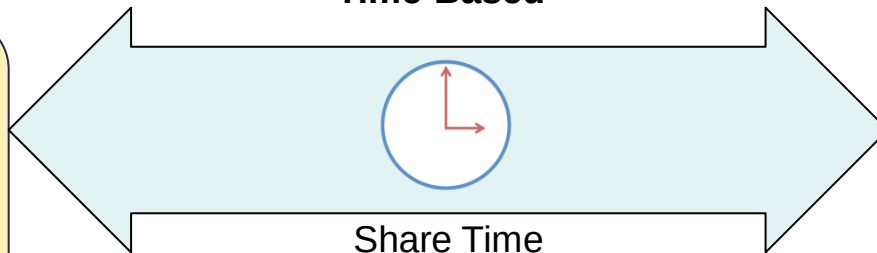
Signal vs. Time-Based Synchronization

Signal-Based



Share Physical Clocks / Triggers

Time-Based



Share Time

Ethernet (1588)

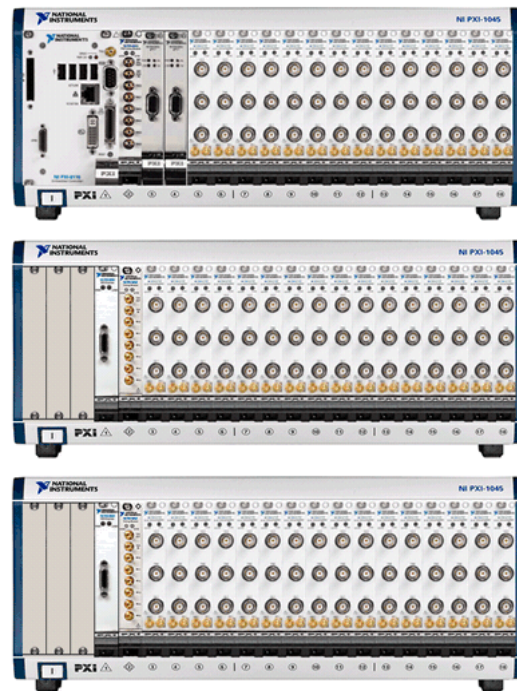
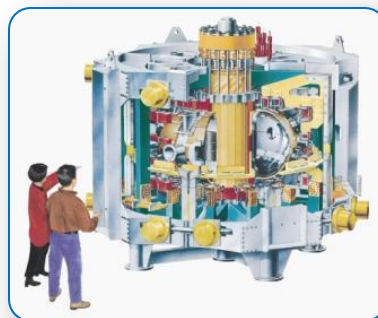
IRIG
GPS
Etc.



Czech Institute of Plasma Physics



- Thomson scattering system
- Synchronized high speed data acquisition
 - 92ch running at 1GS/s
 - Tight synchronization over 3 PXI chassis
 - Skew < 500 ps



M1 Control - Proposed System Setup

**NI cRIO Node for Local
Sensor / Actuator I/O**
• 1 cRIO Node per Mirror

**Deterministic EtherCAT
Network Ring**
• 25-30 cRIO Nodes per
eCAT Network Ring

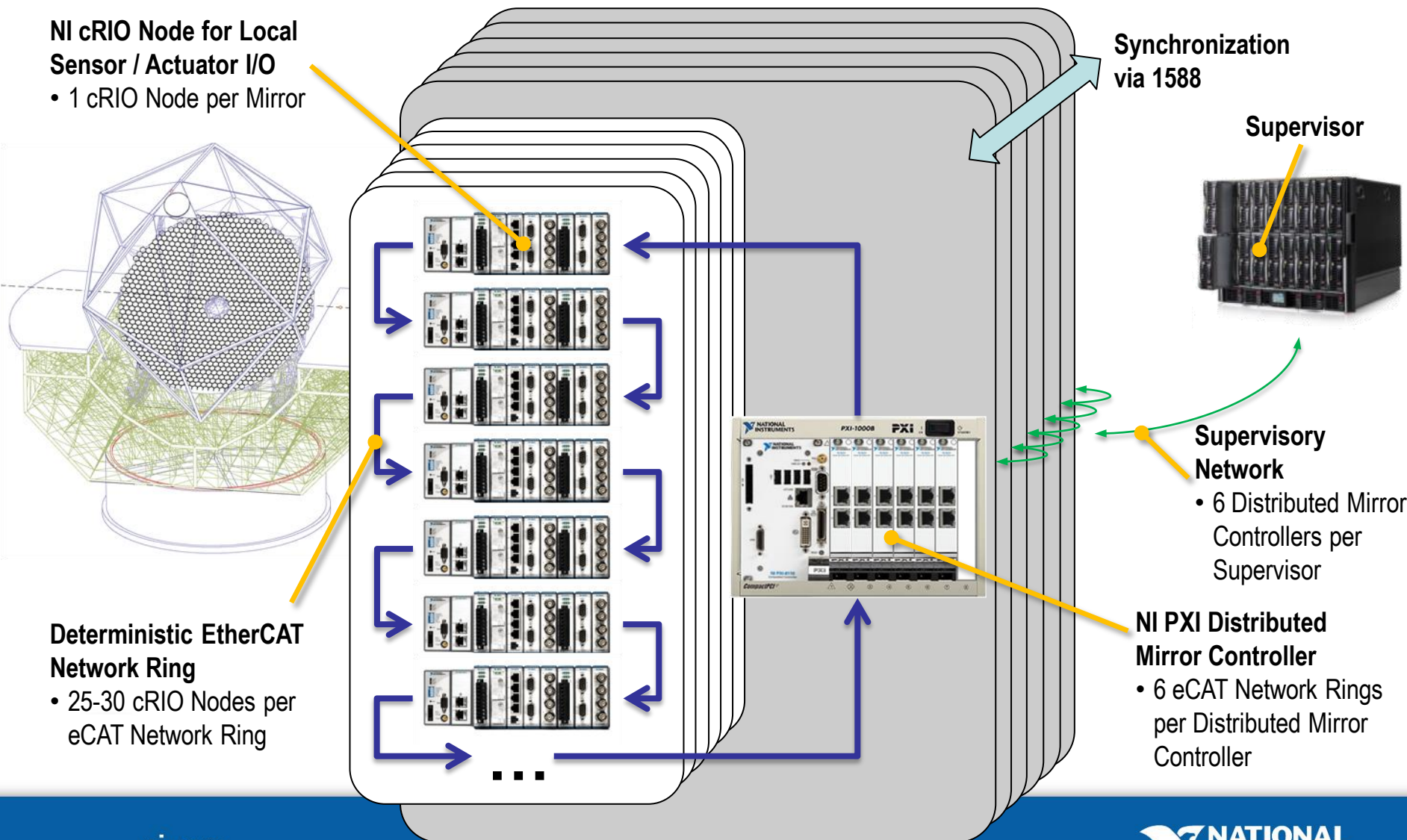
**Synchronization
via 1588**

Supervisor

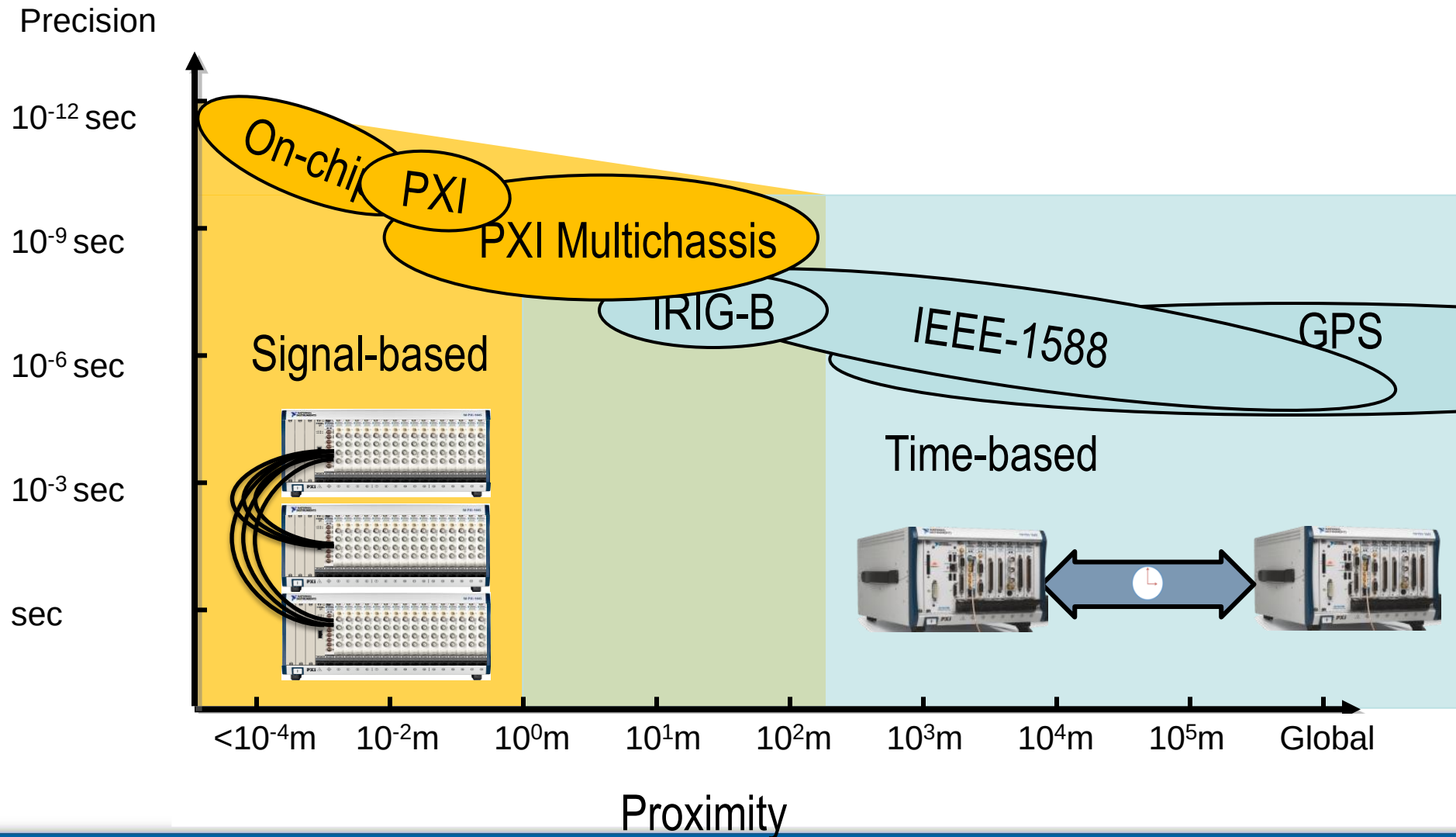
**Supervisory
Network**

- 6 Distributed Mirror
Controllers per
Supervisor

**NI PXI Distributed
Mirror Controller**
• 6 eCAT Network Rings
per Distributed Mirror
Controller



Synchronization Technologies



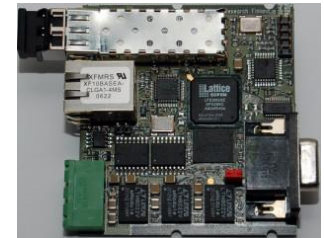
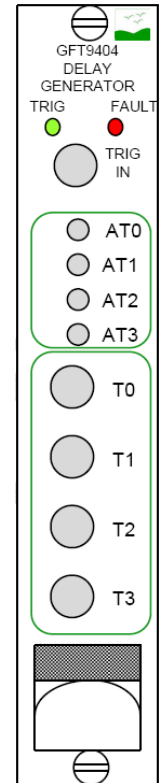
Timing Solutions

- **Greenfield Technology**

- 8 Channel PXI Digital Delay Generator
 - 1ps resolution, <50ps rms jitter
- 4 high precision delays
 - 5ns resolution, <100ps rms jitter
 - Available on the front panel and on PXI Trig

- **Micro-Research Finland**

- PXI Event Generator/Event Receiver
- Working on a cRIO Event Receiver



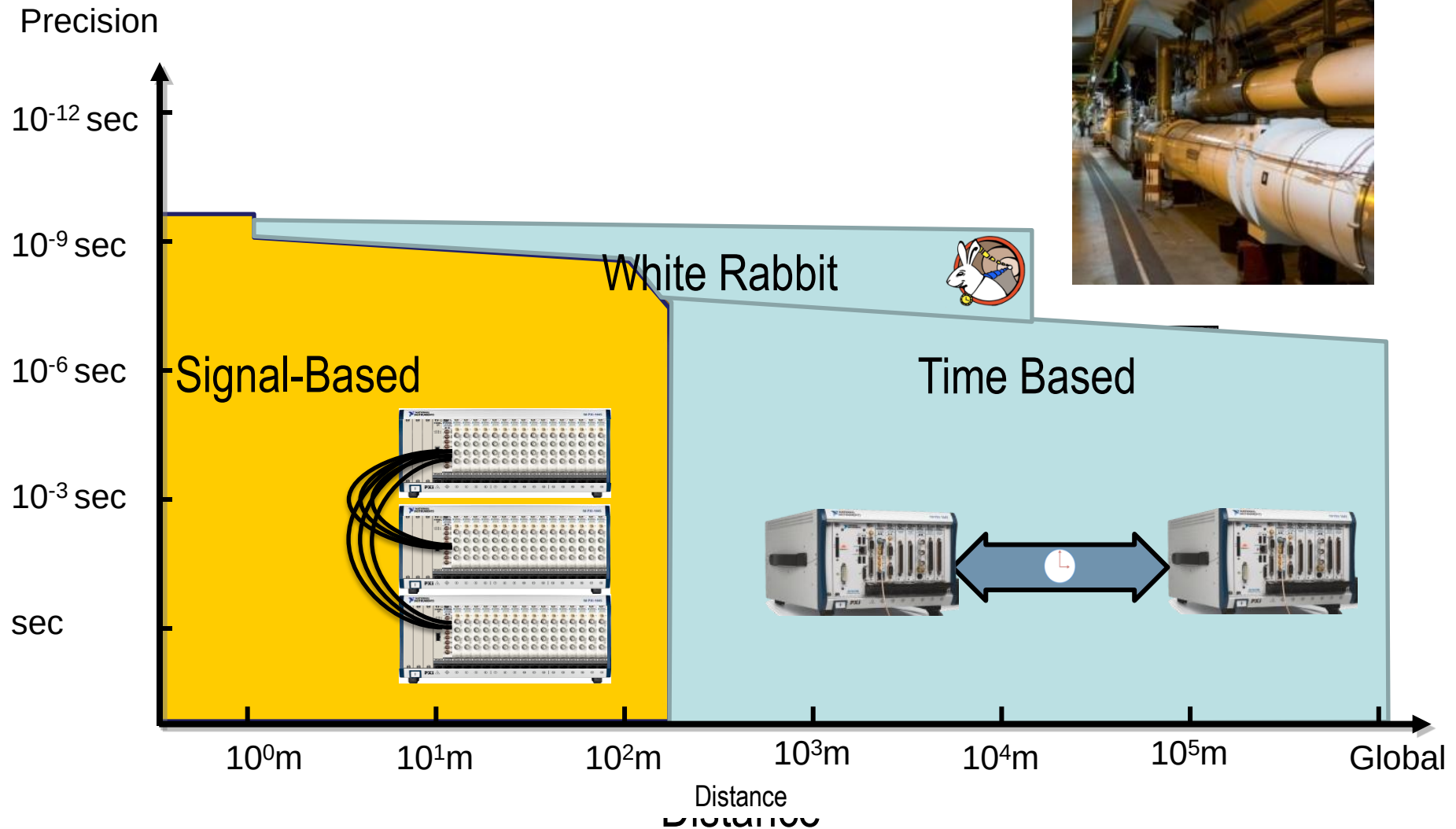
NI and CERN White Rabbit



- Partnering with CERN in developing White Rabbit (WR)
- Performance
 - **Distance:** > 10 km
 - **Scale:** > 2000 nodes
 - **Accuracy:** < 1ns skew, < 100 ps jitter
 - Compensates for propagation delay (cable length, temperature variation, etc.)
- Leverage Industry standards (802.x, **IEEE 1588**, SyncE)
 - Gigabit Ethernet communication with deterministic capability
- Generally Applicable
- Leverage for future PXIe modules

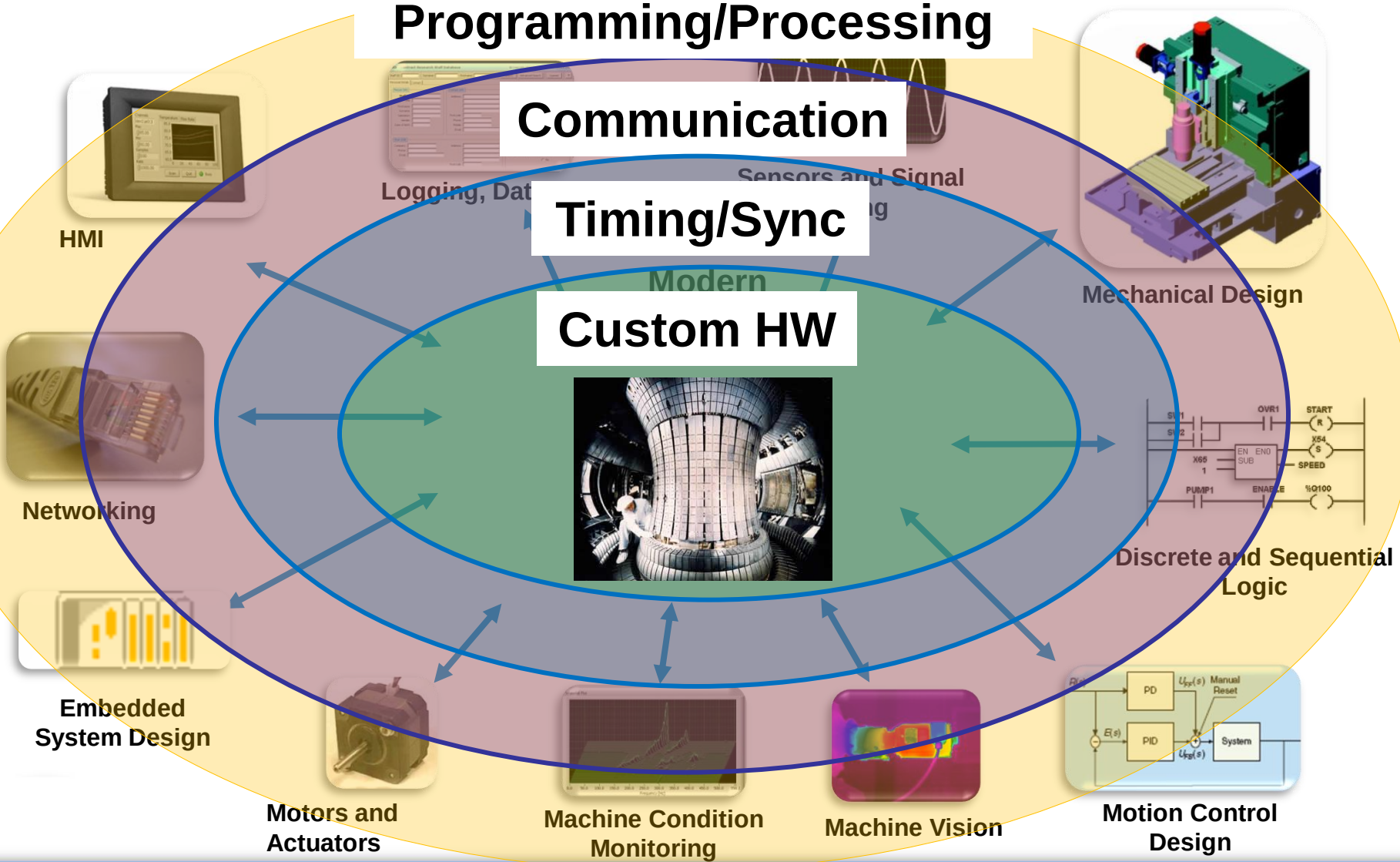


White Rabbit: Synchronization over Distance



Modern System Complexity Increasing

Programming/Processing

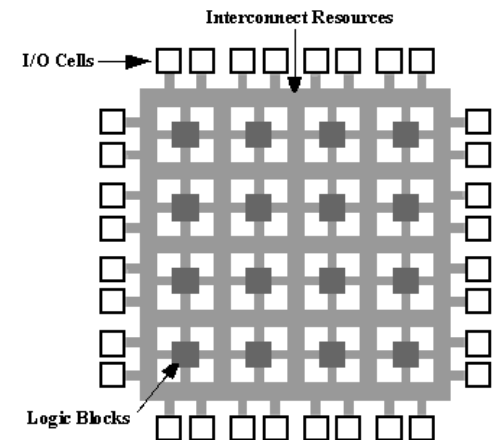


Factors Driving Need for Custom Hardware

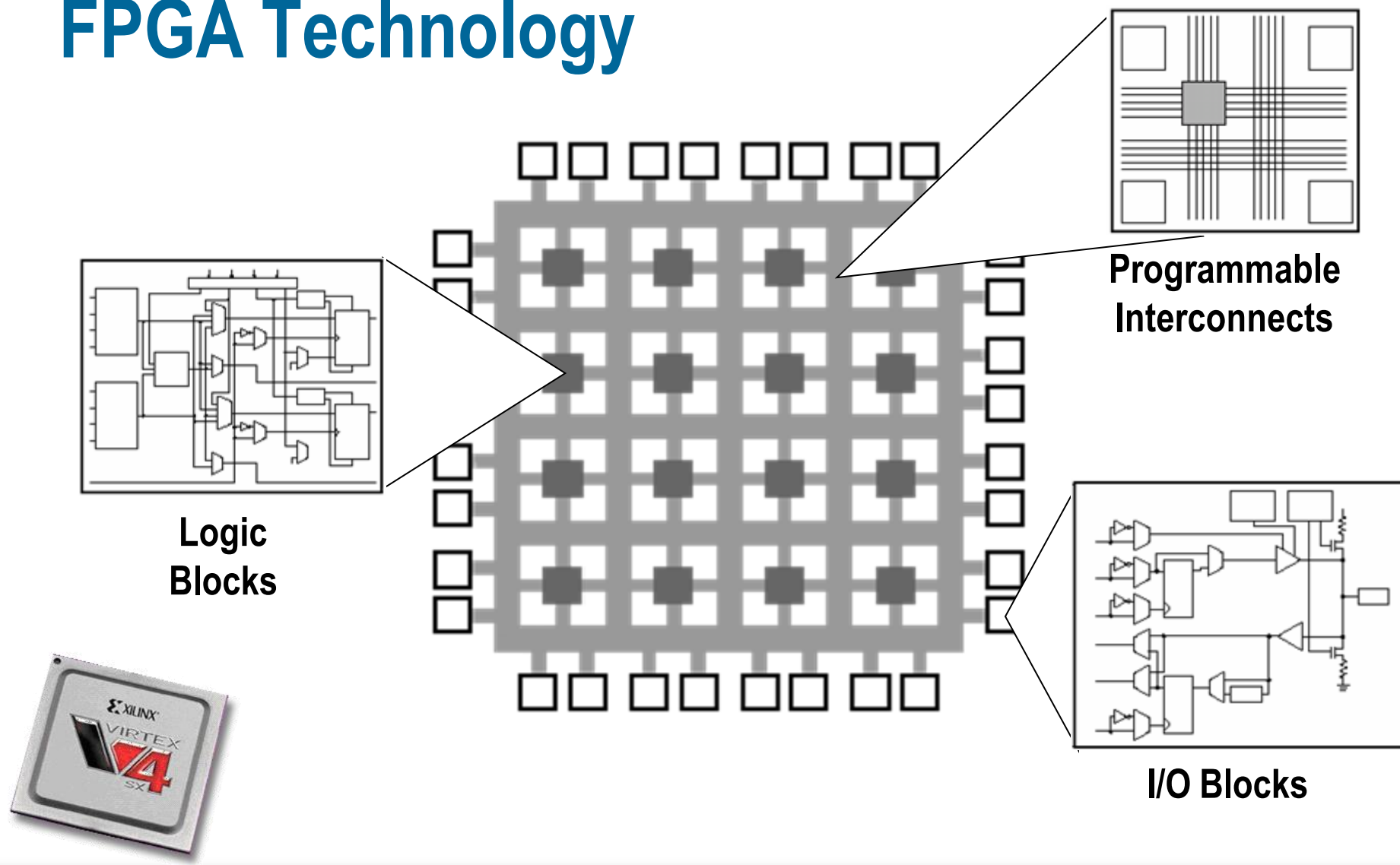
- Very tight control loops
- Onboard signal processing
- Specialized communication protocols
- Custom flexible timing
- Massively parallel processing
- ***REAL NEED: Combination of COTS and Custom!***

Field Programmable Gate Array (FPGA)

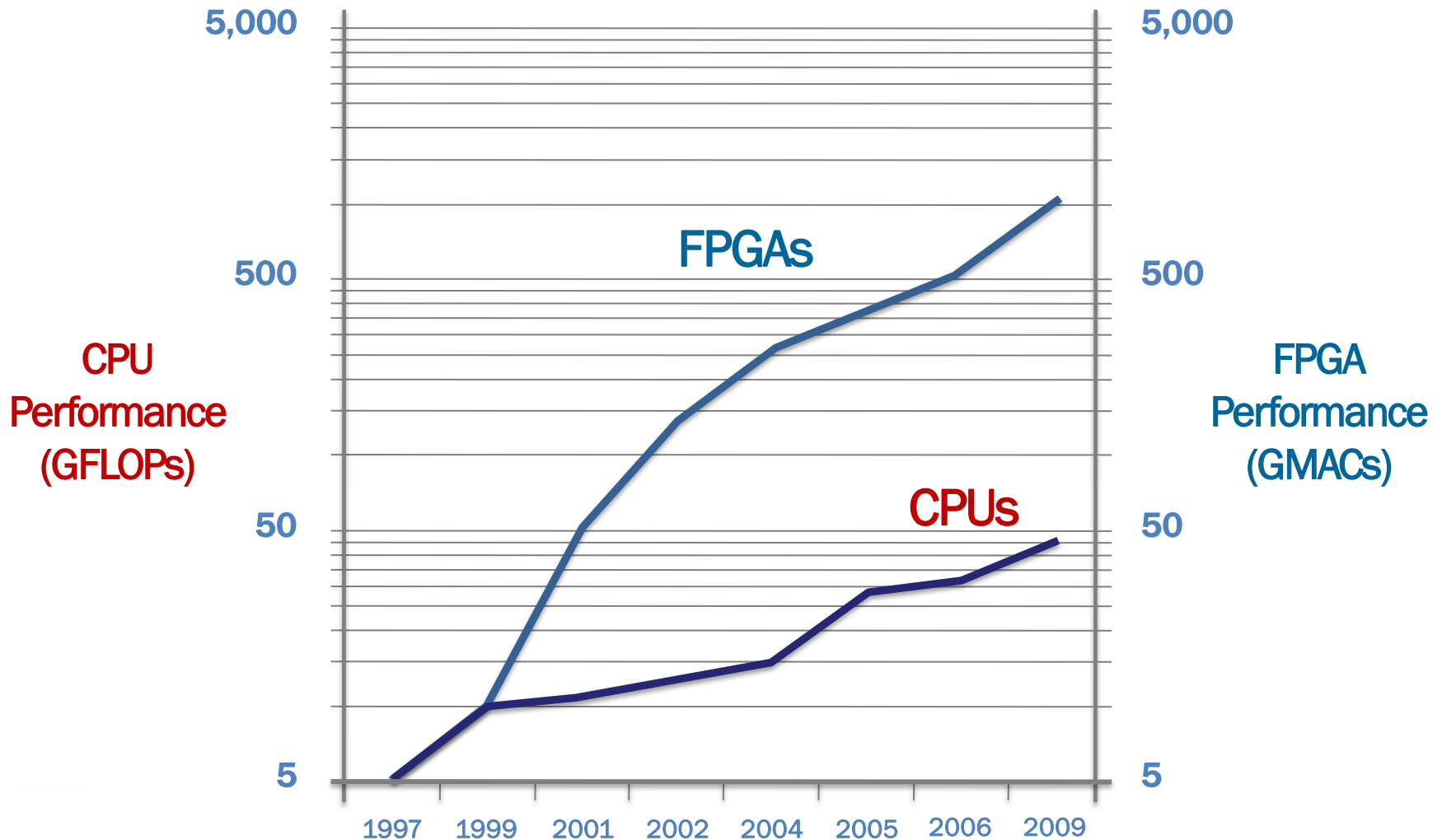
- What it is
 - A silicon chip with unconnected gates/processing resources
- How it works
 - Define behavior in software
 - Compile and download to the hardware
- Advantages
 - Reconfigurable
 - Reliability
 - Parallel execution



FPGA Technology



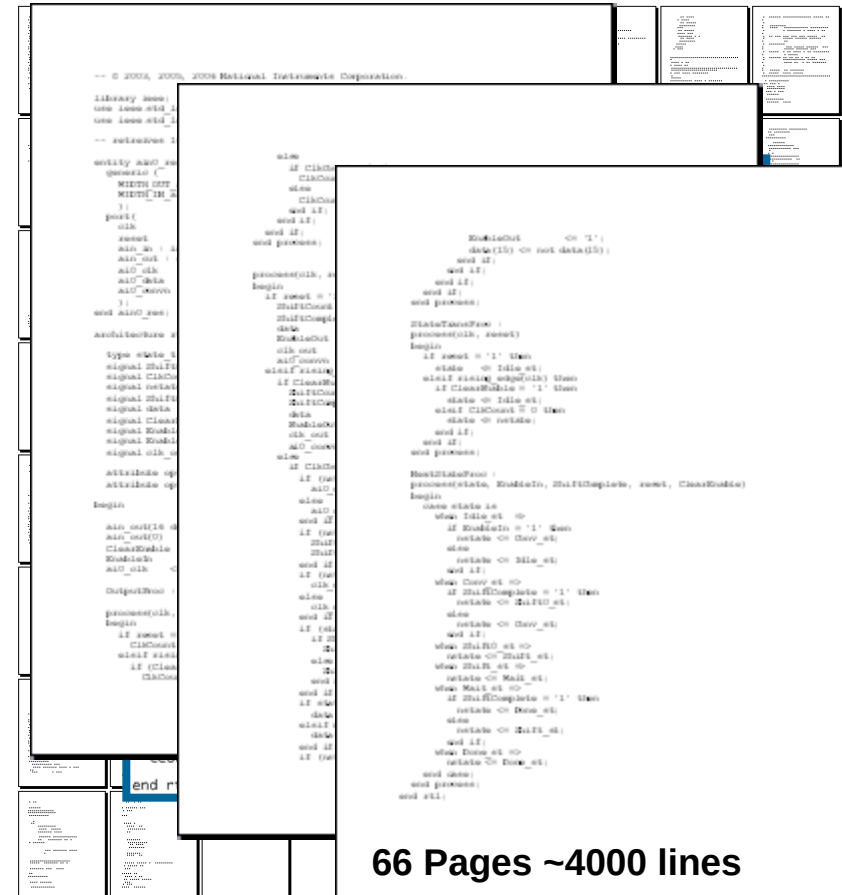
Parallel Architectures Drive Performance



How to Program FPGAs?

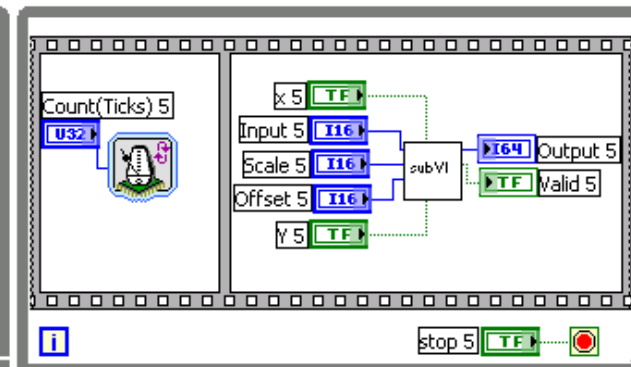
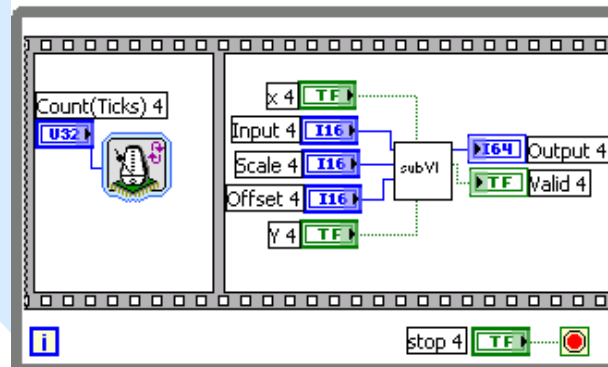
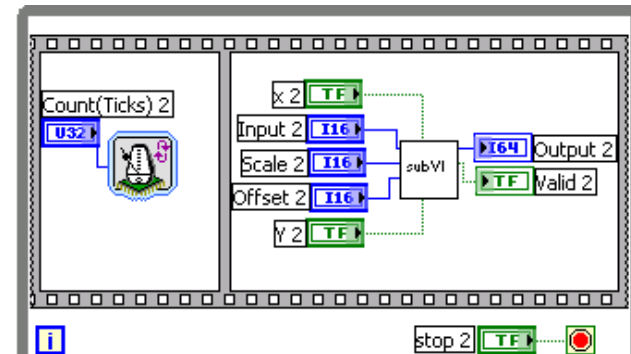
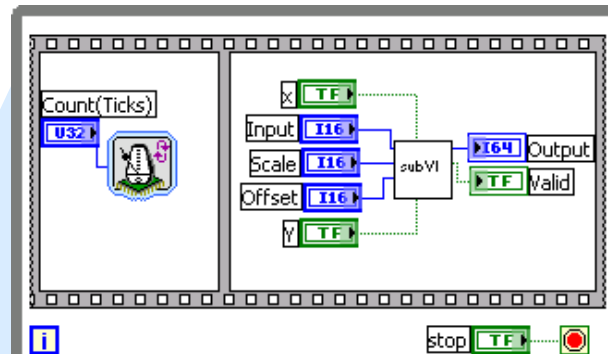
- Schematic capture
 - Graphical depiction
 - Easy to understand
 - Vendor specific
 - Ex: ViewDraw, Ease
- Hardware Description languages (HDL)
 - Text based – “Firmware”
 - Generic or vendor specific
 - Ex: VHDL, Verilog

VHDL



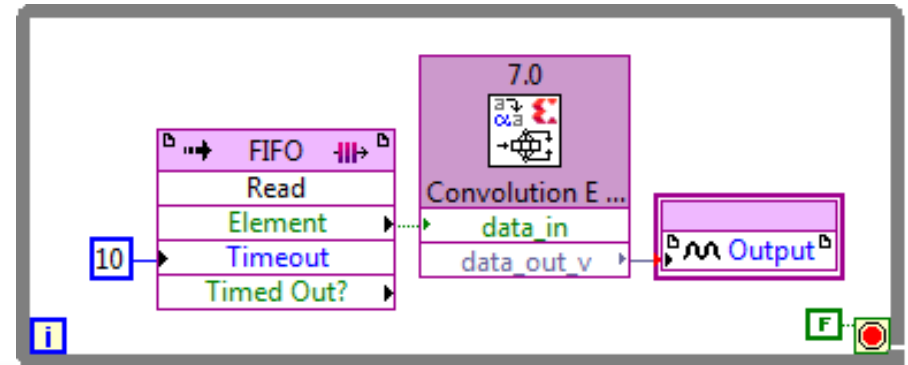
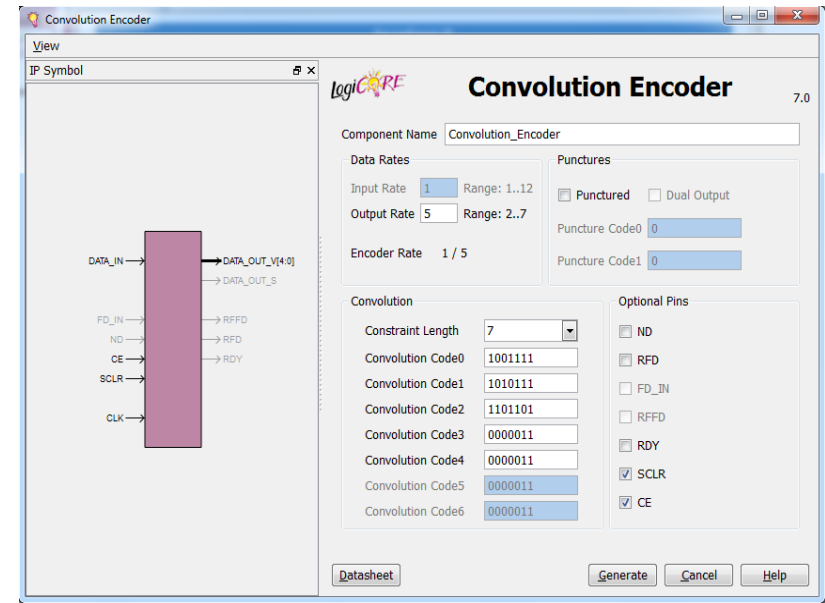
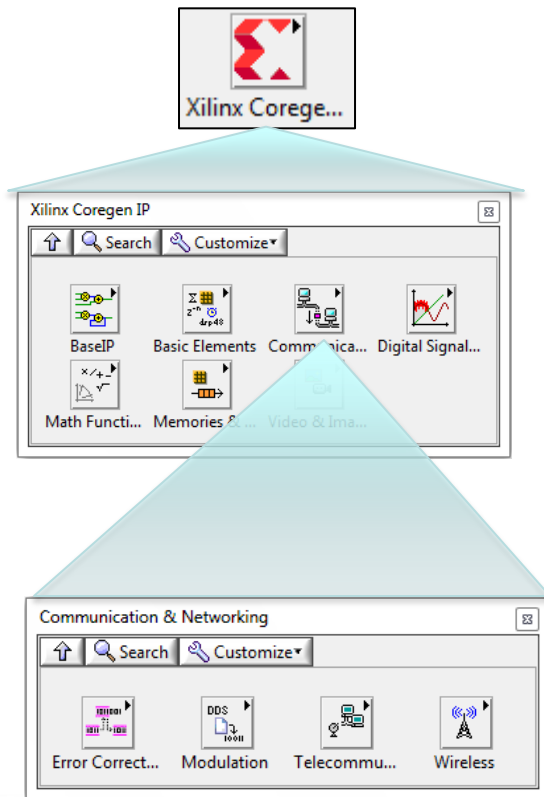
I/O with DMA

FPGA Programming: The Ultimate in Multicore, Multiprocessor Development

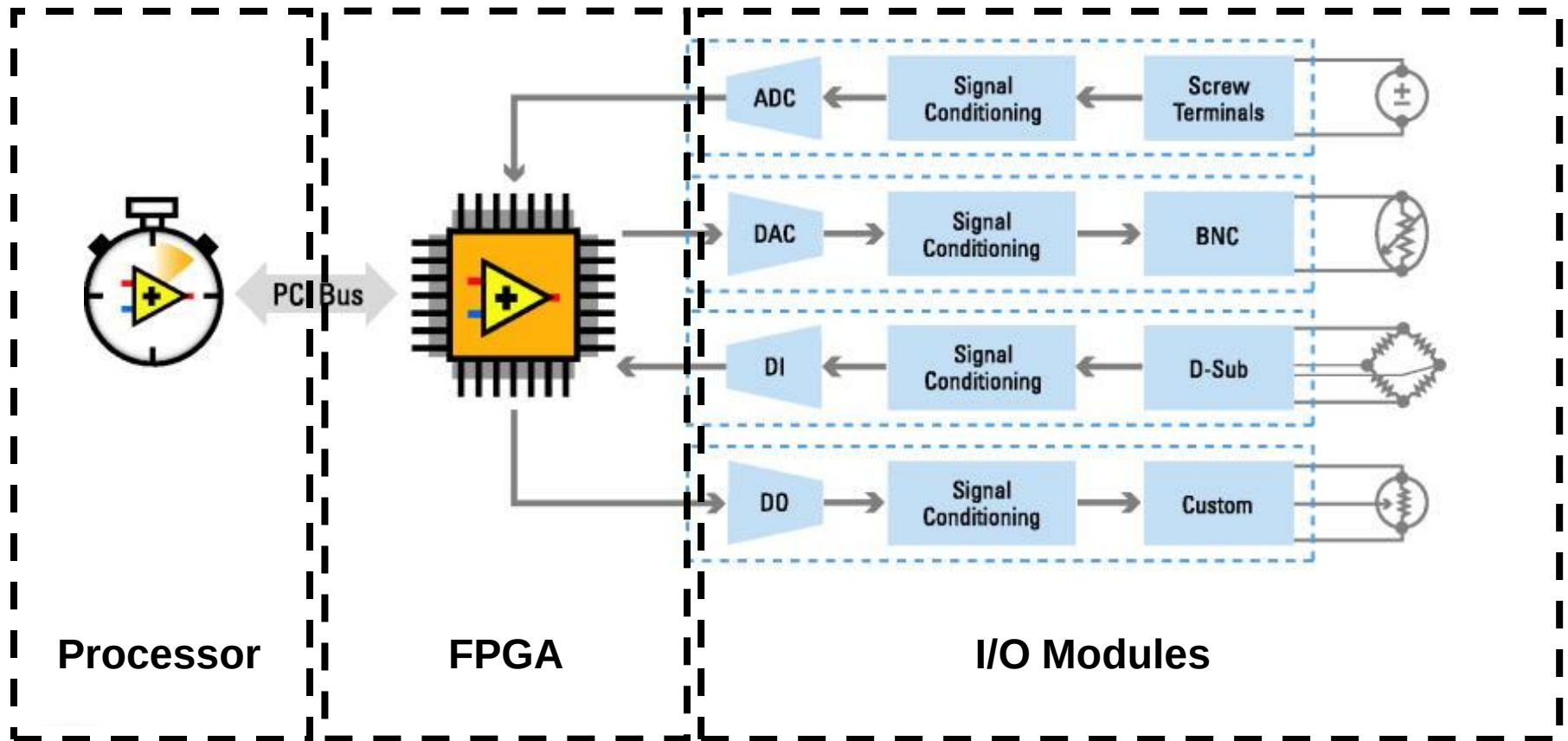


NI Labs | LabVIEW FPGA

Direct Access to Preexisting Xilinx CORE Generator IP Libraries



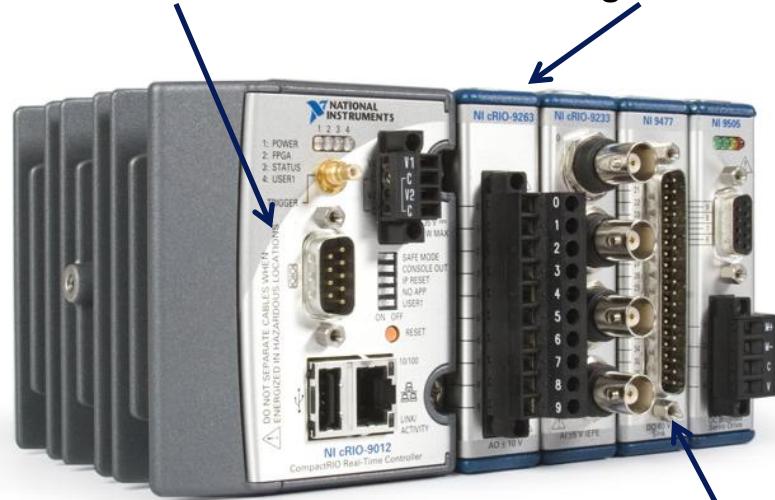
Standard RIO Architecture



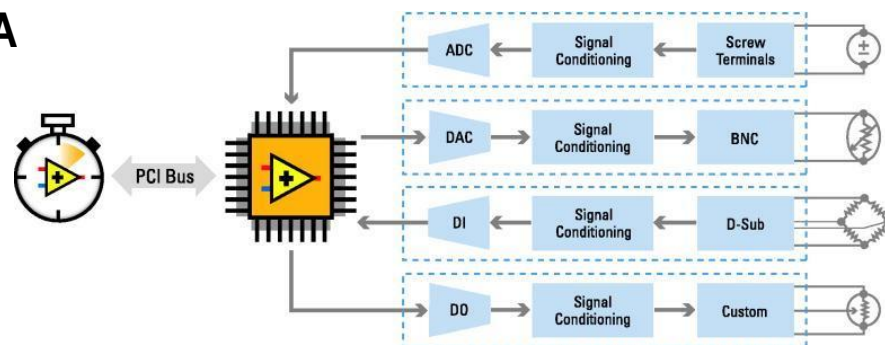
NI CompactRIO

Real-Time Processor

Reconfigurable FPGA



I/O Modules



Extreme Ruggedness

- -40 to 70 °C temperature range
- 50g shock, 5g vibration

Low Power Consumption

- 9 to 35 VDC power, 7-10 W typical

- **I/O Modules** with built-in signal conditioning for connection to sensors/actuators
- **Reconfigurable FPGA** for high-speed and custom I/O timing, triggering, control
- **Real-Time Processor** for deterministic, stand-alone operation, logging and analysis

Over 60 NI and 3rd Party C Series Modules

- **Analog Input**

- Up to 1 M/s, simultaneous sampling
- 4, 8, 16, and 32-ch options
- Built-in signal condition for sensors
 - Strain gages, accelerometers, thermocouples, RTDs
- Up to ± 60 V, ± 20 mA
- 12, 16 and 24-bit resolution
- Available ch-to-ch isolation

- **Analog Output**

- Up to 100 kS/s simultaneous updating
- Up to 16-ch per module
- ± 10 V, ± 20 mA
- Isolation



- **Digital I/O**

- Up to 10 MHz timing
- Counter/timer, PWM
- 8 and 32-channel options
- 5V/TTL, 12/24/48 V logic levels

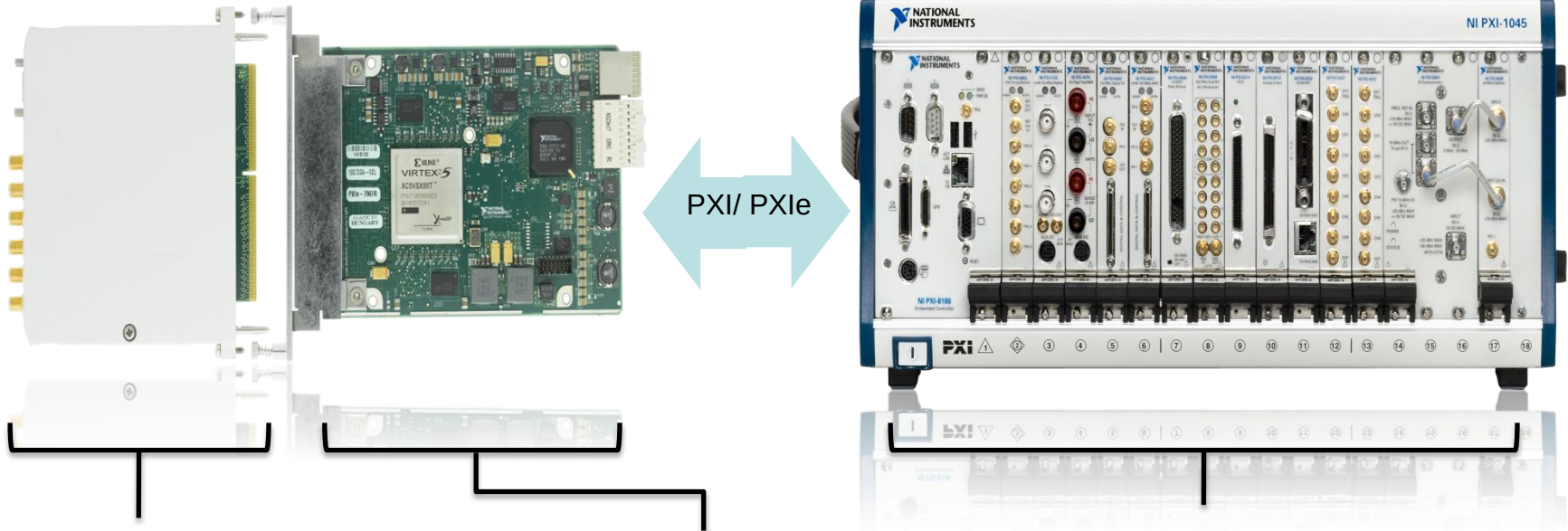
- **Specialty**

- 2-port CAN modules
- Brushed DC servo motor drive

- **Third Party Modules**

- LIN, Profibus, WLAN 802.11, MIL-1553, ARINC-429, GPS, and more

NI FlexRIO



NI FlexRIO Adapter Module

- Interchangeable I/O
- Digital or analog
- NI FlexRIO Adapter Module Development Kit (MDK)

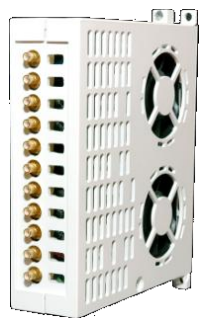
NI FlexRIO FPGA Module

- Virtex-5 FPGA
- 132 digital I/O lines
- Up to 512 MB of DRAM
- Peer-to-peer data streaming

PXI Platform

- Data transfer
- Synchronization
- Clocking/triggers
- Power/cooling

NI FlexRIO Partner Modules



100 MHz
PPMU



Camera Link
and GigE



Multi-gigabit
optical



Dual gigabit
Ethernet

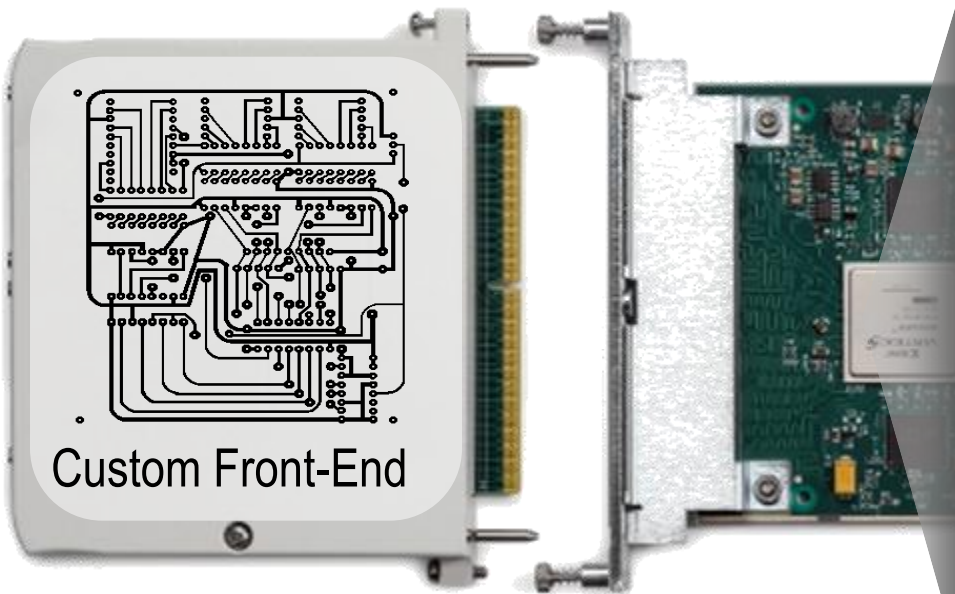


Video and
Automotive

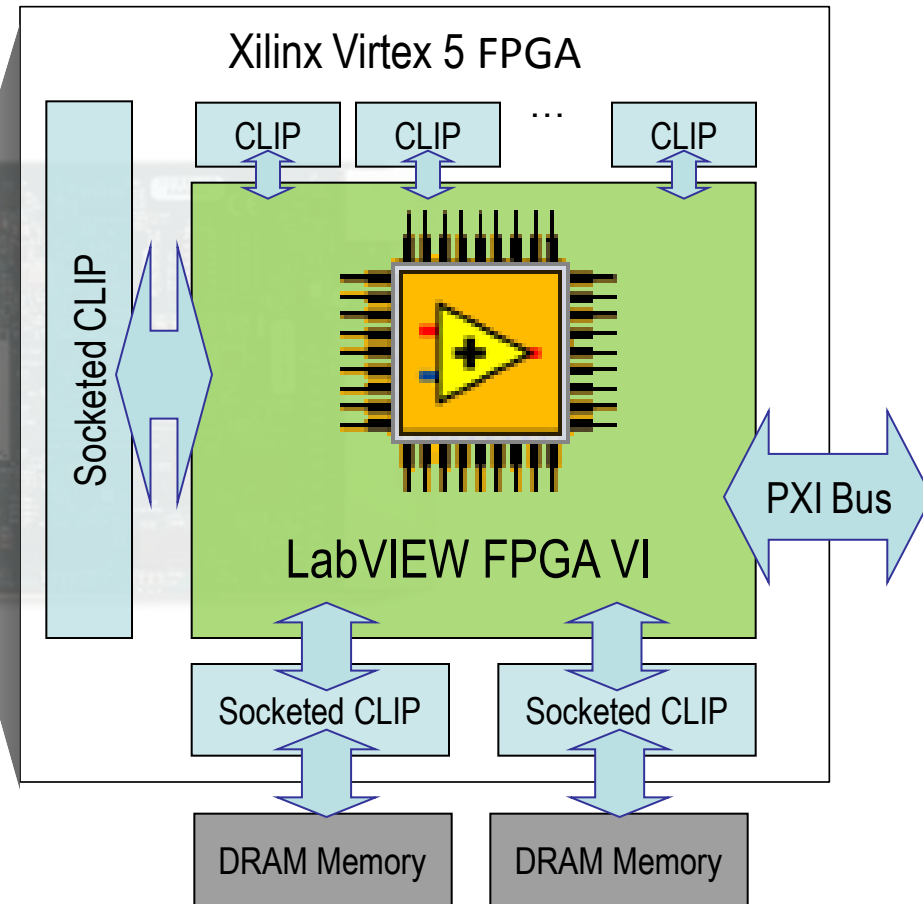


Time to Digital
Convertor

Custom Module Development



Custom Front-End



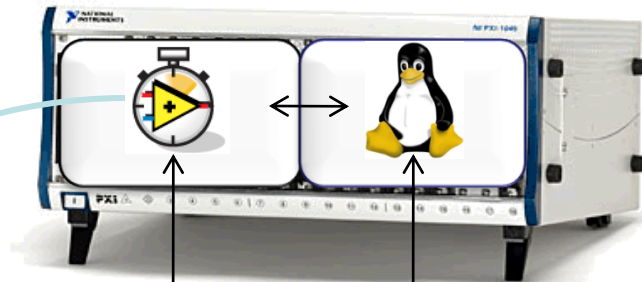
NI Real-Time Hypervisor for Linux

Windows PC



*Must program
LabVIEW Real-Time
application from Windows

Hypervisor System*



Supported RT
I/O



Supported
Linux I/O

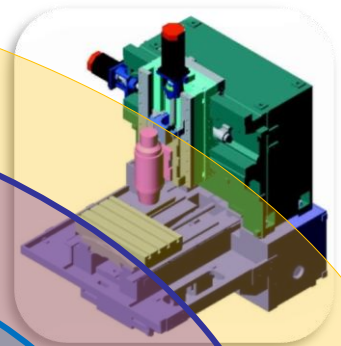


Programming/Processing

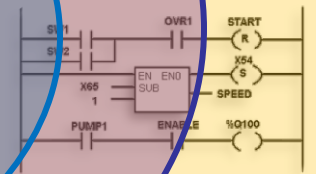
Communication

Timing/Sync

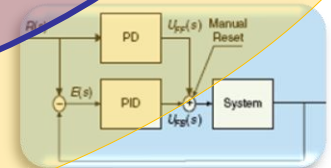
Modern
Custom HW



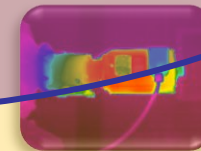
Mechanical Design



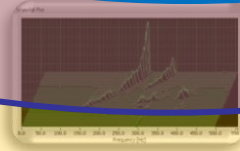
Discrete and Sequential Logic



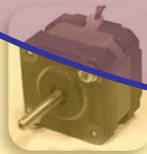
Motion Control Design



Machine Vision



Machine Condition Monitoring



Motors and Actuators



Embedded System Design



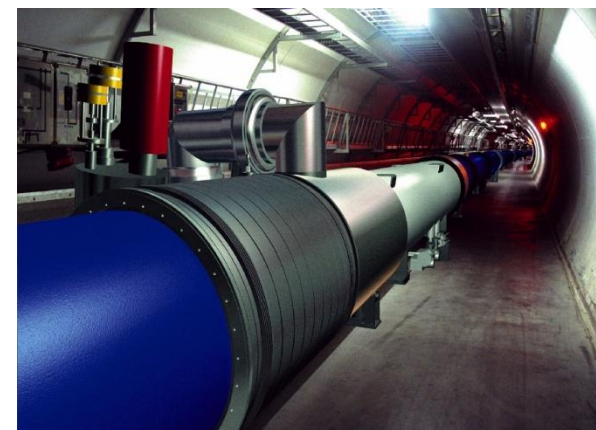
Networking



HMI

CERN Collimator Alignment

- 550+ axes of motion
- Across 27 km distance
- The jaws have to be positioned with an accuracy which is a fraction of the beam size ($200\mu\text{m}$)
- Synchronized to
 - $< 5\text{ms}$ drift over 15 minutes
 - Maximum jitter in μs

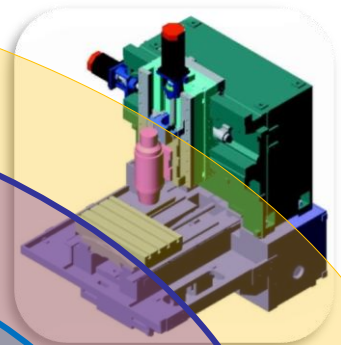


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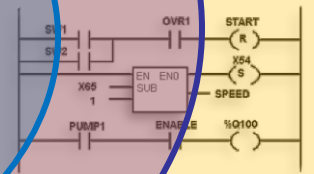
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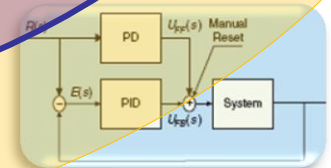
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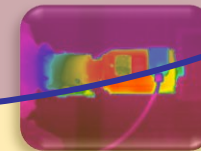
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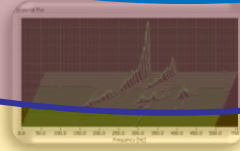
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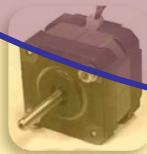
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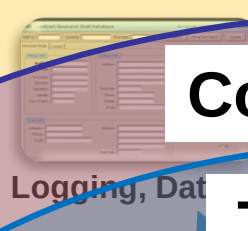
Embedded System Design



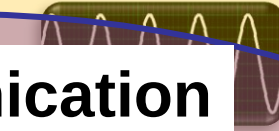
Networking



HMI



Logging, Data



Sensors and Signal

