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DESIGN OF CMOS/SOS CIRCUITS FOR SPACE APPLICATIONS

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I. Abstract

Requirements of integrated circuits for space applications are high speed, small size and great reliability. The CMOS/SOS process technology inherently fulfills these requirements.

Recently discovered problems of reliability are soft errors or "bit-flips" induced by galactic cosmic rays or terrestrial α-particles.

This paper discusses CMOS/SOS circuit design which minimizes these errors. A design example is given for D flip-flop as a typical storage element, and a comparison is made between 4 μm, 2 μm, and 1 μm channel lengths.

Results obtained for short channel lengths indicate that the design of VLSI circuits for space applications with CMOS/SOS technology is feasible and realistic.

II. Introduction

Errors caused by galactic cosmic rays and α-particles radiating from package materials have been reported by many investigators. (1) - (8)

The purpose of this work is to show that by using CMOS/SOS silicon gate technology and by a judicious choice of process and circuit design parameters these error rates can be made very small even for the contemporary and future technologies of very short channel lengths down to 1 μm.

While purer packaging materials can considerably alleviate the α-particle problems, shielding of ICs cannot entirely eliminate cosmic ray induced errors due to the varied nature and high energy spectra of the cosmic rays. (9) Thus careful design of the circuits based on the understnading of the mechanism of error generation is needed. In previous publications models of mechanisms of soft-error generation were proposed for bipolar J-K flip-flop (1) and NMOS dynamic RAM. (10) These models were extended to static CMOS RAMS and PMOS shift registers. (11)

Similarly using an appropriate model for the CMOS/SOS silicon gate technology the cosmic ray induced error rates can be calculated. Calculations involve determination of the minimum deposited energy in the sensitive volume, E_{min}, and of the stopping power, dE/dx, for the critical node of the circuit analyzed. Error rates are then found from the value of the cosmic ray flux of particles which are capable of causing errors. These calculations follow a previously described method. (10) A summary of the method of calculations of error rates is given below:

$$E_{min} = 22.5 \times Q_c \times f \text{ (MeV)} \quad (1)$$

where,

Q_c = critical charge on the sensitive node (picocoulombs)

and,

f = ionization collection efficiency usually assumed 100 percent, hence, $f = 1$

$$Q_c = C_T \times \Delta V \quad (2)$$

where,

$$C_T = C_g + C_m + C_j + C_{ov} \quad (3)$$

$$\Delta V \approx 0.8 \times V_{DD} \quad (4)$$

C_T = total storage node capacitance

C_g = gate capacitance

C_m = metal interconnect capacitance

C_j = p-n junction capacitance

C_{ov} = gate over drain and source overlap capacitance (equals zero for self-aligned gate technology)

V_s = sensitive volume = depletion region of the critical node p-n junction = $w \times t \times h_d$ (5)

where,

w = gate width

t = silicon layer width

h_d = depletion junction width

$$\bar{A}_p = \text{average projected area} = 1/2\,(w \times t + w \times h_d + t \times h_d) \quad (6)$$

$$\bar{S} = \text{average path length} = V_s/\bar{A}_p \quad (7)$$

$$\frac{dE}{dx} = \frac{E_{min}}{\bar{S} \times d_{si}} \quad (8)$$

where,

d_{si} = density of Si = 2.4 gm/cm^3

Using the calculated value of E_{min} and dE/dx the energy ranges of particles capable of causing errors can be found for various groups of particles from Fig. 1. Then, the total flux of particles that can cause errors can be found from Fig. 2 for each group of particles. The sum of these fluxes multiplied by the average projected area gives the error rate, or

$$E_R = \text{error rate} = \phi_{ET} \times \bar{A}_p \times 0.5 \quad (9)$$

The factor 0.5 is due to the fact that error can occur only when "1" is stored which happens 1/2 of the time.

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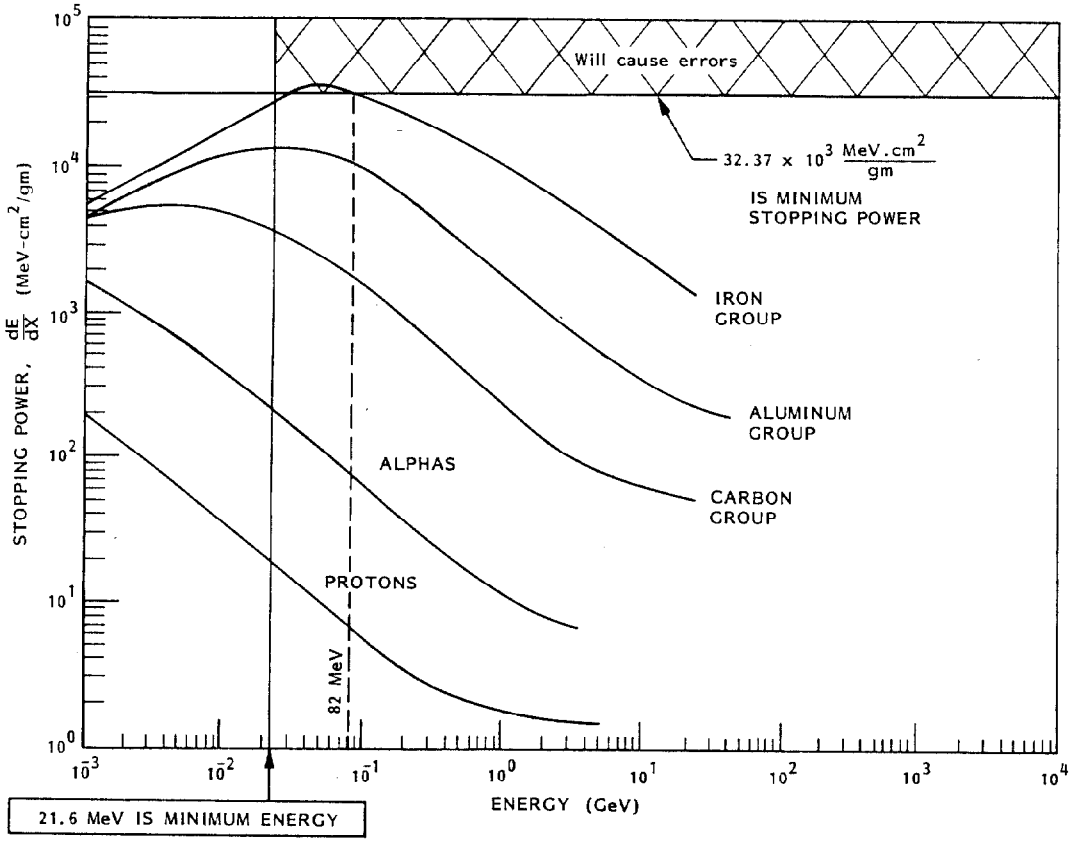


Fig. 1 Stopping power versus energy [5]

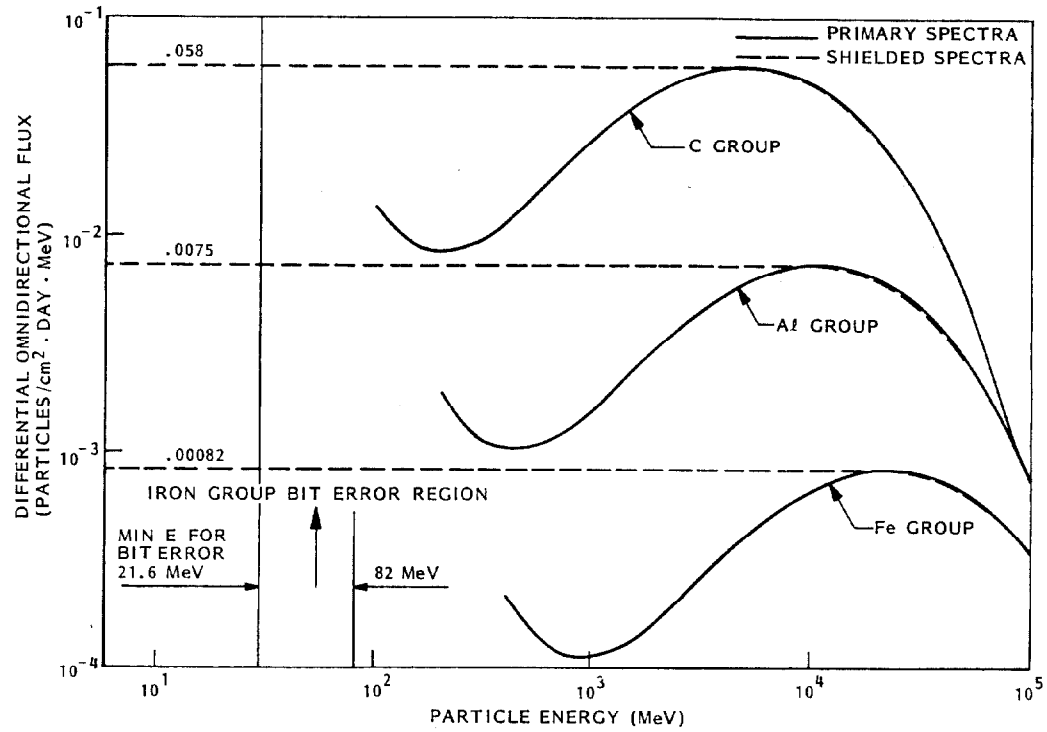


Fig. 2 Estimated differential omnidirectional flux, galactic cosmic rays, Z > 2 [5]

III. Design Considerations

In order to investigate the speed, power consumption, size, reliability and yield of CMOS/SOS process technology three identical circuits were designed with various design rules, namely 4 μm, 2 μm, and 1 μm. These circuits consisted of a 16-bit shift register, input and output buffers, and an input protection network. The basic 1-bit circuit was a D-type flip-flop and is shown in Fig. 3.

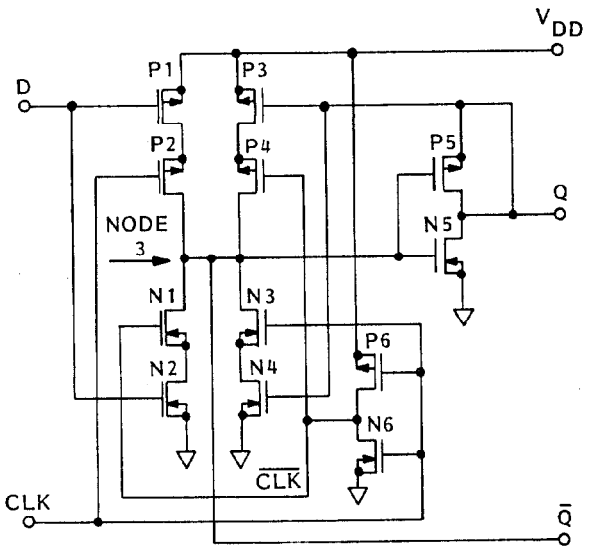


Fig. 3 Circuit of D-type flip-flop

Design of the D-type flip-flop was optimized for the lowest cosmic ray induced error rate without jeopardizing the circuit speed and size. The following design criteria were used:

Storage Capacitance

For a low error rate, high critical charge and hence large storage capacitance are required. In self-aligned gate technology C_{ov} is zero. Metal interconnect capacitance contributes very little to the total capacitance. Junction capacitance depends on the doping concentrations which determines the depletion layer width and on the silicon layer thickness. Neither of these parameters can be manipulated significantly to increase total storage capacitance. Hence, only by making C_g large, could the total storage capacitance be increased. This was done by keeping t_{ox} small and scaling it down for 2 μm and 1 μm designs and by keeping w large.

Device Dimensions, w and l

Channel length, l, is fixed for a particular design, hence w becomes the controlling parameter. Making w large improves the speed and lowers the error rate. The speed is improved because of higher w/l ratio which means lower device "ON" resistance, and the error rate is reduced because with larger w dimension, C_g and C_j both increase, and hence the storage charge increases. Dimension w is limited mainly by chip size and power consumption.

Power Supply, V_{DD}

From expressions (2) and (4), it can be seen that the higher the V_{DD} the larger the storage charge and hence the lower the error rate. A V_{DD} of 10V was chosen for 4 μm design and was scaled down to 7.5V and 5.0V for 2 μm and 1 μm designs, respectively. The supply voltage V_{DD} is limited by device breakdown voltages, by availability and standardization and by power consumption considerations.

Sensitive Volume

Error rate is a function of the sensitive volume. The smaller the sensitive volume, the shorter the average path length and hence the higher the stopping power, see expressions (7) and (8). Now from Fig. 1 it can be seen that higher stopping power reduces the number of cosmic ray particles which can cause error. Thus smaller sensitive volume results in lower error rate provided the storage capacitance is constant. In this design a small sensitive volume was achieved by using SOS process with ion implant for source and drain sufficiently deep to go through the entire silicon island thickness of 0.5 μm, and by making the n-p junction approximately linearly graded which resulted in lower depletion width. Thus the SOS process has an inherently small sensitive volume.

Scaling Factor

For very short channel devices scaling of some parameters is necessary[12]. This usually involves parameters t_{ox}, gate oxide thickness, V_{DD}, power supply voltage and N_A, N_D, doping concentrations. Customarily a scaling constant, K, is taken as the ratio of the channel length of the standard device to that of the scaled-down device. Thus, scaling down from 4 μm design to 1 μm design, for example, would make K = 4. Therefore, t'_{ox}, V_{DD}', N'_A and N'_D of the 1 μm design device should be 1/4 t_{ox}, 1/4 V_{DD}, 4 N_A and 4 N_D of the 4 μm device. This rule was followed for t_{ox}, N_A and N_D, but a reduced scaling factor was taken for V_{DD} in order to keep Q_c high and the error rate low, see expressions (2) and (4). Thus, the values of V_{DD} taken for the 4 μm, 2 μm, and 1 μm designs were 10V, 7.5V, and 5.0V, respectively. These supply voltages should not cause any breakdown problems.

IV. Error Rate Calculations

Cosmic ray induced error rate calculations were carried out for 4 μm, 2 μm, and 1 μm designs. Node 3 of the D flip-flop was the critical node, see Fig. 3. The method followed is outlined in the introduction.

Error Rate of the 4 μm Design

Table 1 shows the parameters used for the design.

Using the parameters from Table 1 and the areas from chip layout shown in Fig. 4, we get

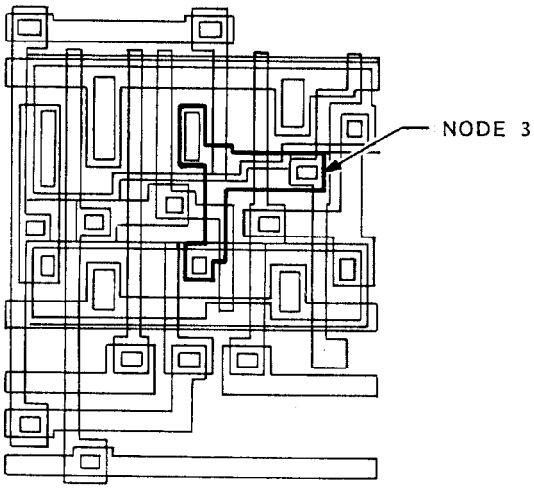
C_g = 0.069 pF

C_m = 0.0340 pF

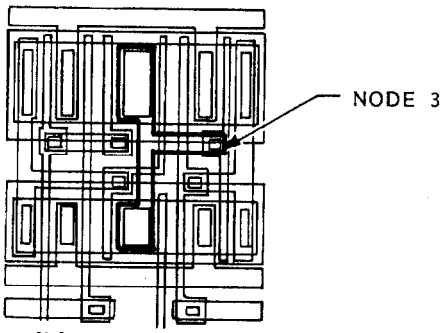
C_j = 0.0170 pF

Table 1 Electrical and physical parameters of the 4 μm CMOS/SOS circuits

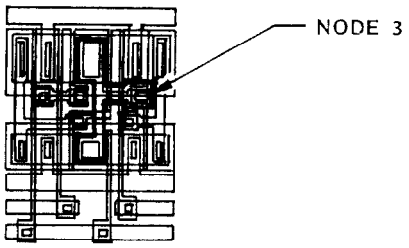
Parameter	Symbol	Nominal Value
Gate oxide	t_{ox}	1050 Å
Silicon island thickness	t	0.5 μm
Depletion region width	h_d	1.2 μm
Side diffusion	h_s	0.1 μm
Gate capacitance per unit area	C_g/A_g	0.34×10^{-3} pF/μm^2
Metal capacitance per unit area	C_m/A_m	0.064×10^{-3} pF/μm^2
Junction capacitance per unit area	C_j/A_j	0.25×10^{-3} pF/μm^2 for p-type 0.52×10^{-3} pF/μm^2 for n-type
Supply voltage	V_{DD}	10V



(a) 4 μm design



(b) 2 μm design



(c) 1 μm design

Fig. 4 Layout of the D-type flip-flop

hence,

$$C_T = 0.12 \text{ pF}$$

and,

$$Q_c = 0.96 \text{ pC}$$

Therefore,

$$E_{min} = 21.6 \text{ MeV}$$

Using the device dimensions of the critical node, we get

$$V_s = 58.8 \ \mu m^3$$

$$\bar{A}_p = 21.1 \ \mu m^2$$

$$\bar{S} = 2.78 \ \mu m$$

hence,

$$(dE/dx)_{min} = \frac{32.37 \times 10^3 \text{ MeV} \times \text{cm}^2}{\text{gm}}$$

With this value of the stopping power only the iron group particles contribute to errors. From Fig. 1 the energy range is 21.6 MeV to 82 MeV, and from Fig. 2 the total flux is:

$$\phi_{ET} = 0.050 \text{ particles/cm}^2 \times \text{day}$$

Therefore, the error rate per device is:

$$E_R = \phi_{ET} \times \bar{A}_p \times 0.5 = 0.53 \times 10^{-8} \text{ errors/day}$$

Error Rate of the 2 μm and 1 μm Design

Similar calculations were carried out for 2 μm and 1 μm designs, except that some parameters were scaled down as follows:

2 μm design, t_{ox} = 525 Å

V_{DD} = 7.5V

1 μm design, t_{ox} = 262 Å

V_{DD} = 5V

Due to scaling, some parameters shown in the Table 1 above were modified as follows:

C_g/A_g = 0.68×10^{-3} pF/μm^2 for 2 μm design

1.35×10^{-3} pF/μm^2 for 1 μm design

C_j/A_j = 0.285×10^{-3} for 2 μm and p-channel

0.594×10^{-3} for 2 μm and n-channel

0.344×10^{-3} for 1 μm and p-channel

0.715×10^{-3} for 1 μm and n-channel

For C_j/A_j calculations a square law relationship of junction capacitance and reverse bias was assumed. The formula used was:

$$C_j/A_j = \frac{C_{jo}}{\left(1 + \frac{V_R}{|\varphi_\beta|}\right)^{1/2}} \quad (6)$$

where,

C_{jo} = junction capacitance at zero bias

V_R = reverse bias across the junction

and

$|\varphi_\beta|$ = absolute value of the bulk junction potential (0.6V was taken at 25°C)

The summary of results is shown in Table 2.

V. Discussion of Results

Considering the design goal of very high speed of operation (above 100 MHz for 4 μm design), the CMOS/SOS circuits for technology and reliability evaluations show a very low error rate. This was achieved by maximizing storage charge and minimizing sensitive volume, without significantly lowering the operating speed. Storage charge was made large by choosing comparatively high power supply voltage and high w/l ratio, which resulted in higher gate and junction capacitances and, at the same time, higher speed of operation. The sensitive volume was made small by using an all ion implant process for depletion through the silicon layer which reduced the depletion region and produced short side diffusion (only due to annealing a approximately 850°C).

Since in the SOS technology source and drain diffusions extend all the way through the silicon layer to the sapphire interface, the depletion region

Table 2 Error rate calculations – summary of results

Parameter	Symbol	Dimension	CMOS/SOS D Flip-Flop		
			4 μm Design Rules	2 μm Design Rules	1 μm Design Rules
Gate capacitance	C_g	pF	0.069	0.052	0.037
Metal capacitance	C_m	pF	0.034	0.027	0.015
Junction capacitance	C_j	pF	0.017	0.015	0.013
Total storage capacitance	C_T	pF	0.120	0.094	0.065
Supply voltage	V_{DD}	V	10.0	7.5	5.0
Critical charge	Q_c	pC	0.960	0.564	0.260
Minimum deposited energy	E_{min}	MeV	21.6	12.7	5.9
Sensitive volume	V_s	μm^3	58.8	45.6	32.4
Average projected area	$\bar{A}_p$	μm^2	21.1	16.5	11.8
Average path length	$\bar{S}p$	μm	2.78	2.76	2.75
Stopping power	$\frac{dE}{dx}$	$\frac{MeV \times cm^2}{gm}$	32.37×10^3	19.17×10^3	8.94×10^3
Energy range	ΔE	MeV	C:0 Al:0 Fe:60.4	C:0 Al:0 Fe:407.3	C:0 Al:142.5 Fe:1792.5
Total error-causing particle flux	φ_{ET}	$\frac{Particles}{cm^2 \times day}$	0.050	0.334	2.54
Error rate for a single S.R. bit	E_R	$\frac{errors}{day}$	0.53×10^{-8}	2.7×10^{-8}	15.0×10^{-8}

of the p-n junctions and hence the sensitive volume are greatly reduced. This reduction, however, results in lower C_j and hence in lower E_{min}, which causes a higher error rate.

The best approach for high speed and good immunity from cosmic ray radiation is to design for a high w/l ratio, thin gate oxide and high supply voltage and to use CMOS/SOS technology with all ion implant deep diffusion process and linearly graded p-n junctions.

VI. Conclusions

Circuits for the evaluation of the speed of operation, power consumption, size, reliability and yield were designed using CMOS/SOS technology. The design was optimized for a low error rate of cosmic ray induced errors. Error rates for three different designs were calculated. These designs had identical circuit schematics, but different design rules and were characterized by channel lengths of 4 μm, 2 μm, and 1 μm. Low error rates obtained for these circuits indicate that the VLSI circuits suitable for space applications can be fabricated with optimized design parameters fully compatible with the contemporary short channel length CMOS/SOS technology.

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