

DESIGN OF A POWER AMPLIFIER FOR THE LAMPF PROTON STORAGE RING TRANSVERSE DAMPER SYSTEM\*

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Summary

A power amplifier has been designed to drive the 50-Ω stripline deflection structures in the transverse active damper of the Los Alamos 800-MeV Proton Storage Ring (PSR). The unit will provide 600-V peak-to-peak with a dc-to-100-MHz bandwidth. Other important characteristics include <40-ns delay time, 50-dB voltage gain, and 4-ns risetime with <5% overshoot and ringing. Because of the current-drive properties of the amplifier, two amplifiers could be combined to provide over 1000-V peak-to-peak into 50 Ω, with very little bandwidth degradation. Components in the power amplifier that represent new designs are a 20-tube distributed-amplifier output stage; a driver stage, using VMOS FET and bipolar transistors; a high-voltage probe, with good dc stability and 150-MHz bandwidth; a transient suppressor circuit, using PIN diodes to protect the transistorized drivers from tube arcing; a nonlinear amplifier to compensate for the nonlinear characteristics of the distributed amplifier; and a first-fail indicator circuit to aid in locating the prime causes of equipment failures.

Introduction

Implementation of the transverse active-damper system for the PSR will require four power amplifiers, two for each axis, to drive the stripline deflection structures. To satisfy the anticipated damper-system requirements, each amplifier will have to meet the following specifications:

Bandwidth (3 db)	20 kHz to 100 MHz
Risetime	4 ns with <5% overshoot and ringing
Output capability	1000 V peak-to-peak into 50 Ω
Transit time	<100 ns
Operating mode	Class A
Power gain	56 db

Other important requirements are operation safety for personnel, high reliability, equipment protection, easy maintenance, and short repair downtime. This paper describes a prototype power-amplifier design that meets most of the design requirements outlined above.

The amplifier design described has the following characteristics:

Bandwidth	dc to 100 MHz
Risetime	4 ns with <5% overshoot and ringing
Output capability	600 V peak-to-peak into 50 Ω
Delay	<40 ns
Operating mode	Class A
Power gain	50 db

Although a single amplifier module does not meet the full output capability nor the power gain requirements listed for the final design, two such amplifiers can be combined to meet these requirements with only a slight modification to bandwidth and risetime properties. Several new circuit designs were necessary to produce the prototype power amplifier shown in the block diagram of Fig. 1.

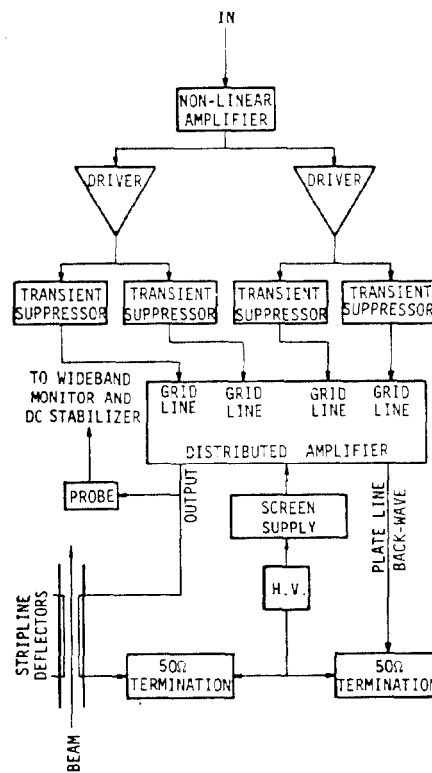


Fig. 1. Power amplifier simplified block diagram.

Distributed Amplifier

The high-power, wide-bandwidth output capability is provided by a 20-tube distributed amplifier using water-cooled RCA 4636 tetrodes that were designed specifically for distributed-amplifier<sup>1</sup> use. This circuit is made of ten sections, each section using two tetrodes with their plates paralleled (Fig. 2). The plate and grid lumped-transmission lines use negative mutual-inductance for linear phase, wide bandwidth, and parasitic tube inductance compensation. The RLC circuits labeled Xp and Xg in Fig. 2 reduce the high-frequency ringing with very little effect on risetime. This ringing is reduced even further, at the expense of increased risetime, by delaying the grid drive signal to one pair of grid lines. The optimum delay for greatest ringing reduction is one-half the ringing-frequency period. Figure 2 shows a waveform obtained when using these ringing-reduction techniques. To obtain maximum output capability from the distributed amplifier, it is necessary to select the screen voltage for each tube because the RCA 4636 tetrodes have considerable tube-to-tube variation. These voltages are obtained from a Zener-diode string, powered by the plate supply. To protect the tetrodes from destructive arcs, a 20-ns SCR circuit is used to crowbar the screen voltages when an arc is detected. The plate supply is also fast crowbarred, but with a 10-μs SCR.

Drivers

Generally in the past, it has been necessary to use a second distributed amplifier to drive wideband distributed-amplifier output stages. Transistorized

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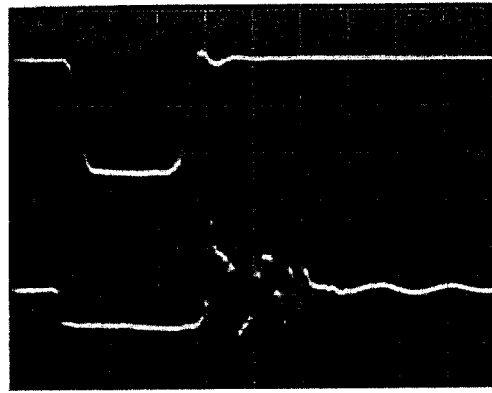
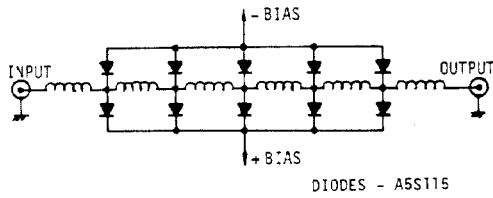


Fig. 4. Transient-suppressor simplified schematic and pulse-limiting waveform.

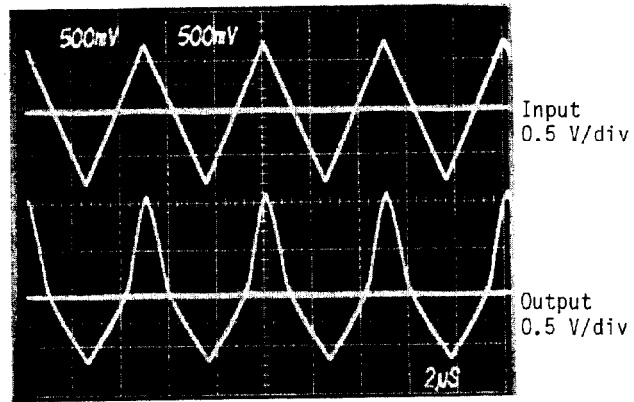
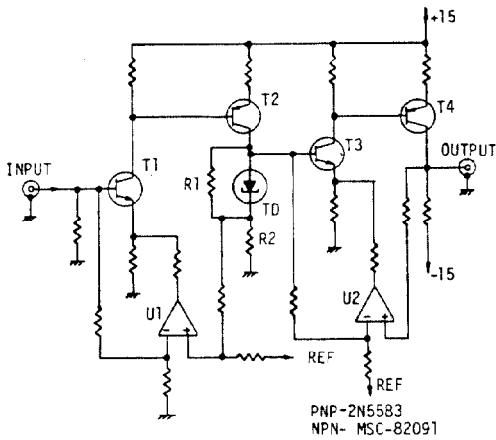


Fig. 5. Nonlinear-amplifier simplified schematic and waveforms.

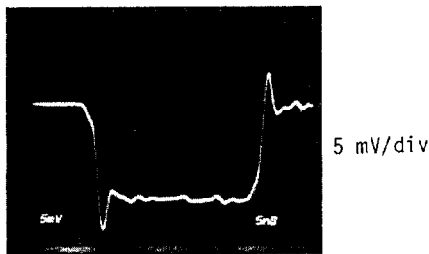
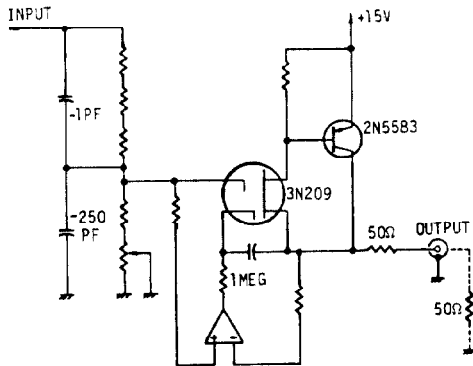


Fig. 6. High-voltage probe simplified schematic and pulse response.

### First-Fail Circuit

To aid in locating prime causes of equipment failure, a first-fail circuit has been designed. This circuit monitors all interlock functions and indicates the first function that fails during an equipment shut-down. This should greatly reduce trouble-shooting time in many instances. The circuit uses multichannel MHTL latch circuits.

### Acknowledgments

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### References

1. E. Ginzto, W. R. Hewlett, J. H. Jasberg, J. D. Noe, "Distributed Amplification," Proc. of the IRE, 36, No. 8, pp. 956-969 (1948).