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BEAM PHASE LOCK USING AMPLITUDE LIMITED PULSE COMPARISON FOR THE ZERO GRADIENT SYNCHROTRON (ZGS)*

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Summary

Solid state high frequency limiter amplifiers and fast rise time voltage comparators for pulse shaping make zero crossing time a meaningful phase reference. A circuit based on these principles was developed and is in use in the beam phase feedback loop of the ZGS. It has excellent linearity for voltage out vs delay for up to 50° with a phase error of < 8° for the following input condition: input voltage amplitude from 0.1 - 2.0 V and beam bunch rate from 4.4 - 14.0 MHz. A detector is included to insure a zero output reference when there is no beam or when beam levels are below the phase-lock threshold.

Introduction

Phase angle stabilization is achieved by comparing the phase of a signal from a beam induction electrode with the phase of the RF cavity voltage. The error signal from the phase detector then drives the voltage-controlled master oscillator frequency, in the direction to reduce the error.

The vacuum tube phase feedback unit, which was originally used, had performed satisfactorily until recently when it began to have intermittent failures. The system was quite complex since it included heterodyning (beat frequency) circuits so that all phase comparison was done on 1 MHz signals. Research began several years ago in the use of solid state circuits for pulse shaping and zero crossing time comparison, in place of the phase discriminator. A limiter amplifier with discrete components was first tried, but had too long delay time. Since the upper fundamental bunch rate is 14 MHz, we are concerned with rise times of $< 0.35/14$ MHz $= 0.025$ μs. The faster the rise time of the amplifier, the better defined is the zero crossing time. The required integrator output frequency response is determined by the highest synchrotron frequency, which is 11 kHz for the ZGS.

Circuit Description

General

Figure 1 is a diagram of the most recent circuit. An RCA CA 3012 integrated circuit amplifier, designed for limiter use, works well for our application. The amplifier has a gain of 1,000 with an upper frequency cutoff of 20 MHz. The voltage comparator, which is the zero crossing detector, uses discrete components. It has a rise time of 10 ns. Care was taken with all the high speed circuits to prevent transistor saturation and minimize delay. The signal from the induction electrode is amplified by a vacuum tube preamplifier at the electrode, to insure a reasonable signal-to-noise ratio. A minimum signal amplitude of 0.1 V is needed at the input of the limiter amplifier for good operation.

Figure 2 contains a timing diagram which will help to explain the logic of the system. The delay time for the beam signal and the RF should be the same for optimum operation and minimum correction from the feedback system. The stable phase angle for the ZGS is 150° on the RF cycle, which means the beam current peaks at this value. Due to the fact that the RF polarity is inverted at the detector and that the physical location of the pickup electrode with respect to the cavity gives a -25° phase shift (see Fig. 3), the total phase shift appears as in Fig. 2. Figure 4 shows the waveform at the output of the voltage comparator No. 1 for a 0.2 V, 14 MHz sine wave input. The dc average of the output from the ac coupled limiter represents the correction signal. The "OFFSET" control at the ac coupled limiter output is used to reference the desired phase angle to zero output.

The symmetry of the circuit with respect to both inputs reduces effects of errors in zero crossing time. This is because both channels will have similar error and give a cancelling effect. Note that the flip-flop and ac coupled limiter perform the same function as the discriminator in the usual detector.

No Beam Interlock

Provision is needed to insure that the phase feedback is not driving the master oscillator with a strange corrective signal at the time the RF is bunching the beam, prior to acceleration. This protection is achieved by the flip-flop and the ac coupled limiter. If either input has less amplitude than needed to trigger the flip-flop, it remains in a stable state, and the limiter output remains at zero.

Performance

Figure 5 gives a plot of phase error vs frequency for equal inputs of 2 V and 3 - 15 MHz. Also shown is a plot for Input 2 voltage attenuated by 12 dB. The data were determined by using a frequency sweep generator.

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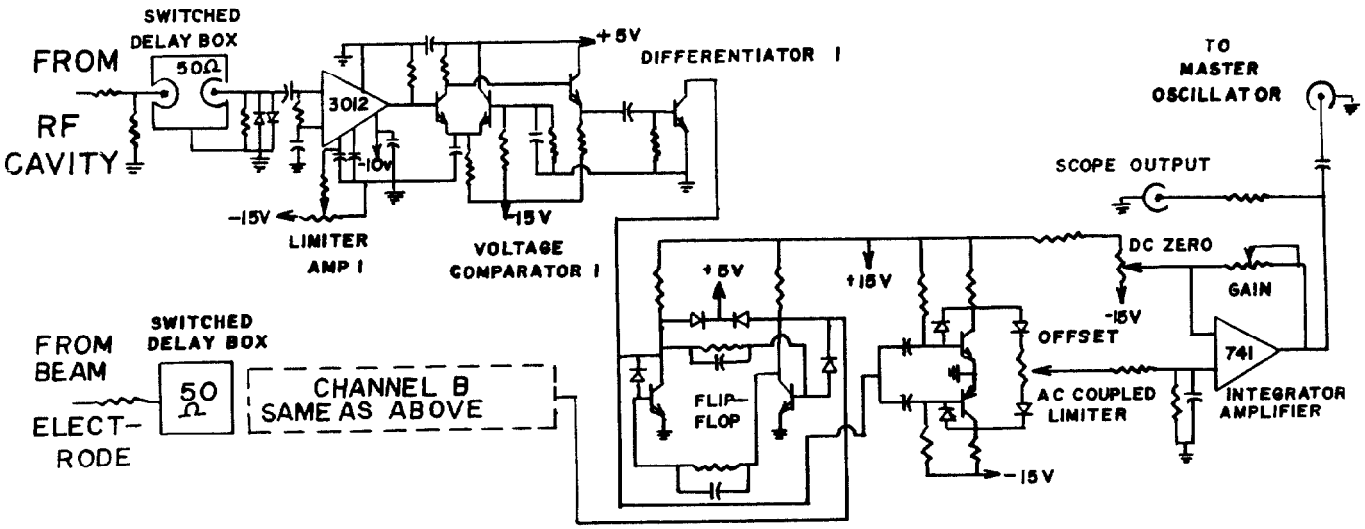


Fig. 1 Circuit Diagram of Phase Control

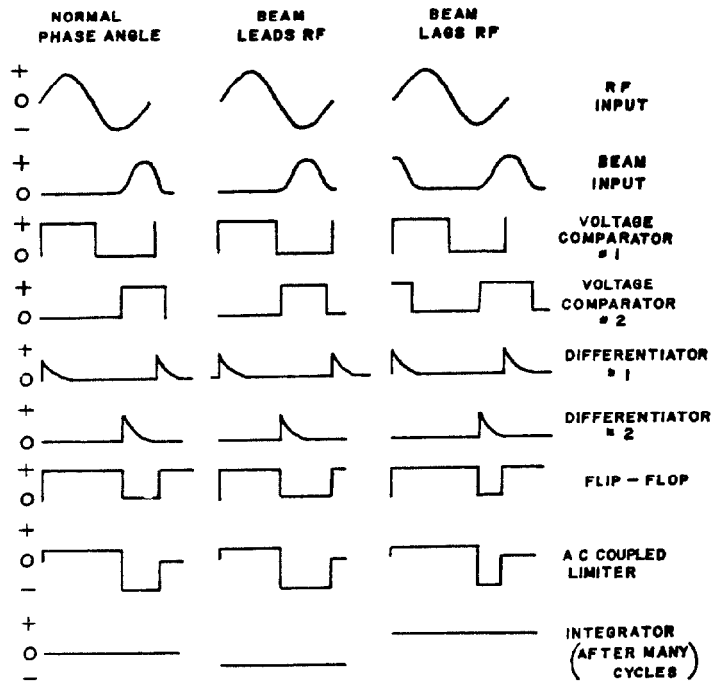


Fig. 2 Timing Diagram for Possible Inputs

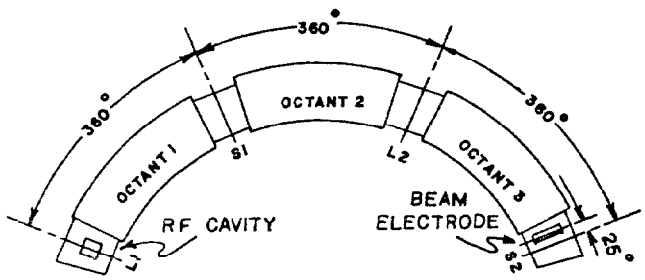


Fig. 3 Signal Pickup Locations. ZGS has Eight Octants and Operates on the Eighth Harmonic

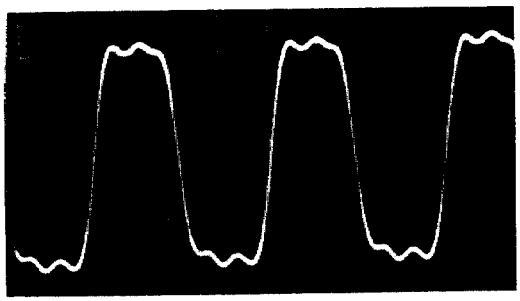


Fig. 4 Output of Voltage Comparator 2. Input 0.2 V, 14 MHz Sine Wave

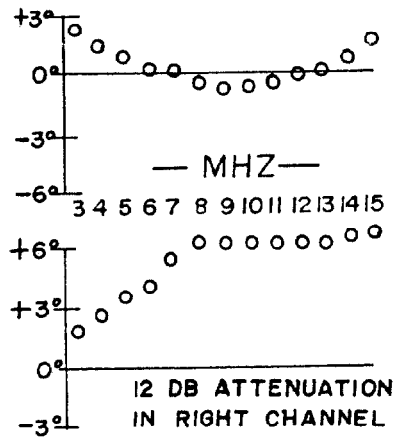


Fig. 5 Phase Error vs Frequency for 2 V at Both Inputs. (Upper Graph.) Lower Graph: One Input Attenuated