ISBN: 978-3-95450-214-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2021-TUPAB389

# HIGH PRECISION FOUR QUADRANT CONVERTER WITH GaN TECHNOLOGY

M. Incurvati*, T. Margreiter, R. Stärz, MCI INNSBRUCK, Innsbruck, Austria
T. Riedler, National Taipei University of Technology, Taipei, Taiwan

*Abstract*

New proton therapy facilities for the cure of tumors as well as high energy photon sources are currently being installed all around the world. In this field the request for special power supplies for corrector, scanning and quadrupole magnets are increasing. For these applications, mandatory requirements are high bandwidth and current stability as well as low output ripple which are conflicting constraints. A feasibility study, prototype development, measurements, and investigations on the control methodology of a wide bandgap GaN semiconductor-based power module is presented in the paper. The developed power module features the following characteristics: Eurocard standard PCB, bi-polar 4Q operation, minimum switching frequency 100 kHz, control bandwidth 5 kHz, output voltage and current up to 200 V / 8 A output current ripple < 20 ppm. The enlisted characteristics make it suitable for high inductive loads requiring fast transients (scanning magnets). An RST controller will be developed and a system identification approach to the transfer function of two parallel connected power modules will be presented along with simulations assessing the performance.

## INTRODUCTION

Particle accelerators for research and medical applications are in need of highly accurate power supplies for corrector, scanning and quadrupole magnets. Key requirements for such power supplies are high bandwidth, high current stability and a low current ripple. As the bandwidth is realized by high DC-link voltages and high output filter bandwidth, this leads to higher switching frequency demands for keeping the current ripple low. For avoiding increased losses with the given prerequisites, the new semiconductor technology gallium nitride (GaN) promises to fulfil these requirements better compared to conventional silicon switches. The target is to assess the performance with the latest 600 V CoolGaN™ technology of Infineon. To deploy the full advantage of this technology, the design of driver and fast current circuit has to be accomplished highly deliberate. Additionally, the closed loop performance of a simulated solution is assessed to have a prediction for operation with scanning magnets.

## REQUIREMENTS AND HW-SIMULATION

The target is to design a DC-DC converter with integrated output-filter and EMI-filter, capable of four-quadrant operation and specification as summarized in Table 1. The PCB is intended to be mounted in a 19" rack, therefore the layout is based on the Eurocard standard.

Table 1: Specifications of One Inverter Board

| Parameter | Value |
|---|---|
| DC input voltage | 150 - 200 V |
| output voltage | DC / AC |
| max. load frequency | 5 kHz (sinusoidal) |
| max. load current | 8 A RMS per board |
| max. load current ripple | 20 ppm peak-to-peak |
| switching frequency | ≥ 100 kHz |
| load inductance | 400 µH - 4 mH |
| switching topology | hard-switching full-bridge |

The PWM signals are provided externally, measurements for current and voltage are on-board. The principle diagram is shown in Fig. 1. There, it can be seen that the PWM signals for the two boards are 180° phase shifted in the carrier signal, in order to enable an interleaved operation for lowering the output current ripple.

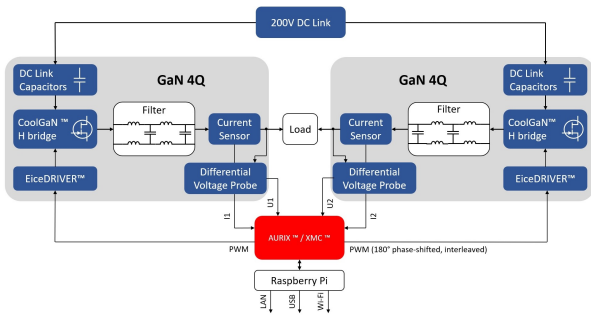


Figure 1: Schematic of two GaN 4Q boards connected to one load in interleaved mode.

For best switching performance the driver circuit is of major importance and is therefore adapted from the Infineon half-bridge evaluation platform EVAL_1EDF_G1_HB_GAN, with fully isolated EiceDRIVER™. The basic layout for the output filter was adopted accordingly [1]. The filter, a fourth Order Bessel-Design, has a damping stage after the second LC stage and a desired break frequency of 10 kHz. The actual filter layout is shown in Fig. 2.

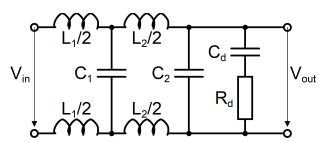


Figure 2: Schematic of the output filter with split up inductors.

* Maurizio.Incurvati@mci.edu

ISBN: 978-3-95450-214-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2021-TUPAB389



## PROTOTYPE AND HW-TESTS

As mentioned, the driver circuit for the appropriate performance of the inverter is crucial. Second key point is the fast switching current-path between DC-link capacitors and the switches of its leg. To reduce switching losses caused by voltage overshoot, the parasitic inductance of this loop has to be kept as low as possible. The resulting design is shown in Fig. 3 and is based on a reference design [2].

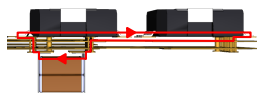

Figure 3: DC-link loop with fast switching current-path (labeled in red).

The first prototype for investigation with mounted heat sink is shown in Fig. 4. Its performance analysis is done with a purely resistive load (12 Ω / 300 W) and due to the high slew rates, a KEYSIGHT DSOS204A scope with a bandwidth of 2 GHz is utilized.

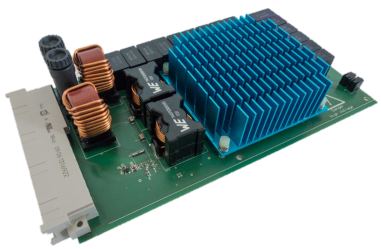

Figure 4: GaN 4Q prototype with mounted heat sink.

## CONTROLLER SIMULATIONS

The simulation conducted in SIMULINK can be seen in Fig. 5. The voltage trajectory reference for the controller is generated by means of a triangular signal generator operating at the desired triangular current frequency. The power converters are driven by means of interleaved modulation as explained in Fig. 1. From this simulation, also the transfer function for the open loop plant is derived within MATLAB and it is of 9 $^{\text{th}}$-order. The simulation period is 10 ns.

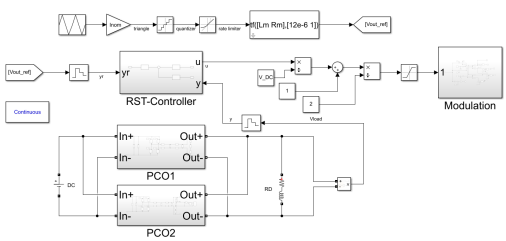


Figure 5: Simulation of two converter boards in interleaved modulation with voltage reference generation.

## RST-CONTROLLER SYNTHESIS

The synthesis process for the applied RST controller follows the methods utilizing Diophantine equations [3]. Recalling that the identified plant transfer function, called $G_p(z)$ can be factorized with

$$G_p(z) = \frac{B^- B^+}{A^- A^+}. \tag{1}$$

Where $B^-$ and $A^-$ contain all unstable zeros and poles that lie outside or on the border of the unit disk. In contrast, $B^+$ and $A^+$ contain the poles and zeros to be kept as a choice of the designer.
In order to obtain a desired static gain, the numerator of the desired closed loop transfer function called $B_m$ has to contain all zeros with insufficient absolute or relative damping, thus they must divide the numerator. Therefore, $B_m$ has to be rewritten as

$$B_m = B^- B'_m. \tag{2}$$

A polynomial called $A_m$ is responsible for imposing the desired 2 $^{\text{nd}}$-order dynamics by means of specifying the bandwidth $\omega$ and damping $\zeta$. Furthermore, the controller in its canonical form is shown in Fig. 6.

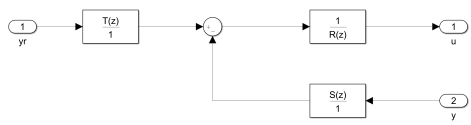


Figure 6: RST-controller implementation in SIMULINK, where yr is the reference, u the controller output and y the system feedback.

From the previous statements and considering the controller structure, the equation to be satisfied can be written as

$$\frac{B\,T}{A\,R + B\,S} = \frac{B^- B'_m}{A_m A_o}, \tag{3}$$

where $R, S$ and $T$ are the controller polynomials to be determined. With the mentioned factorization, simplification and considering that $R$ and $S$ of Eq. (3) have to be expanded with $R = B^+ R'$ and $S = A^+ S'$, Eq. (3) can be rearranged. Hence, the so called primary and auxiliary Diophantine equations from the numerator and denominator terms can be stated, where the former reads as Eq. (4a) and the latter as Eq. (4b).

$$A^- R_1 R' + B^- S_1 S' = A_m A_o \tag{4a}$$

$$T = B'_m A_o \tag{4b}$$

Closer inspection reveals that Eq. (4a) is of the form

$$A(s)C(s) + B(s)D(s) = q(s), \tag{5}$$

which is known as a Diophantine equation and can be solved by setting up a Sylvester matrix [4]. Solving the resulting linear system of equations and extracting the unknown $R'$ and $S'$ polynomials from the variable vector provides a unique solution. Since $R$ and $S$ can now be computed, the $T$ polynomial has to be determined, according to the auxiliary Diophantine Eq. (4b) by means of $B'_m$ and setting $A_o$ to 1.

ISBN: 978-3-95450-214-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2021-TUPAB389

## RESULTS

With the first test runs the performance of the overall system including driver, switches and filter is verified. The design of the switching current path is validated at 150 V input voltage and shows an overshoot of 14% and an undershoot of 23% of $V_{DS}$. The result for the rise- and fall-times of $V_{DS}$ from a bottom switch at 100 and 150 V $V_{DC}$ is shown in Fig. 7. It can be observed, that the rise time is decreasing with increasing DC-link voltage. The dynamics are very competitive and even faster than stated in the data sheet of the switch [5].

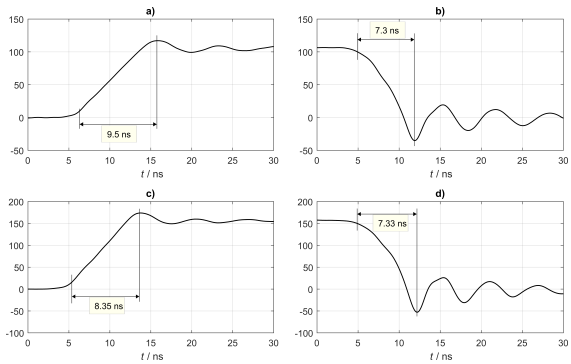


Figure 7: a,c) Rising and b,d) falling edge of $V_{DS}$ / V of a bottom switch, at $V_{DC}$ = 100 V (a,b) / 150 V (c,d).

With a power temperature calibration, the real power losses are compared to the calculated. Out of measurements a connection between electrical losses and temperature increase can be found. Subsequently, operating the inverter in normal switching mode (AC-mode), the measured temperature increase gives an estimation of actual losses. The results for this comparison are shown in Table 2. The calculated losses for the switches are about the same as the indirect measured by the calibration. The losses for the inductor $L_1$, in contrast, are almost twice the calculated. Reasons for this could be the thermal linkage between the switches and inductors, an incorrect model for the losses calculation or losses due to harmonics.

Table 2: Parameters and Results for Power to Temperature Calibration at Two Different Operating Points

| Parameter | OP 1 | OP 2 |
|---|---|---|
| $V_{IN}$ | 200 V | 200 V |
| $I_{IN}$ | 0.55 A | 2.38 A |
| $V_{OUT}$ | 35.1 V | 73.6 V |
| $I_{OUT}$ | 2.9 A | 6.1 A |
| Efficiency | 93.3 % | 94.8 % |
| Losses of GaNs in AC-mode | 5.5 W | 12.5 W |
| Losses of GaNs calculated | 4.6 W | 12.2 W |
| Losses of Ind. $L_1$ in AC-mode | 1.7 W | 3.7 W |
| Losses of Ind. $L_1$ calculated | 0.9 W | 1.8 W |

The output filter design is evaluated by measurements of the output voltage ripple and they are showing the same amount of voltage ripple as expected from simulations. Ultimately, the simulated closed loop wave-forms are presented in Fig. 8a) and 8b). The achieved and utilized parameters are summarized in Table 3. The shown nominal peak current $I_{nom}$ is ±15 A. The step current $I_{step}$ is 5% of $I_{nom}$. In order to determine the reason for the present time delay, further investigations are required.

Table 3: Parameters and Achieved Closed Loop System Performance for Two in Interleaved Modulation Simulated Power Converters. Values Acquired from Simulation Results

| Parameter | Value |
|---|---|
| $\omega$ | 10 kHz |
| $\zeta$ | 1 |
| Regulation frequency | 40 kHz |
| Rise time | 100 µs |
| Settling time | 250 µs |
| *P.O.* | 0.05% |
| Steady state error | 500 µA |

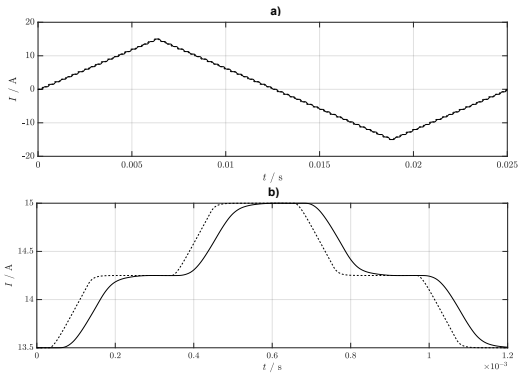


Figure 8: Simulated closed loop current wave-forms, with the load (solid) and the reference current (dashed). a) ramp and staircase waveform of the simulated current within one cycle period. b) close up to the staircases.

## CONCLUSION

The designed and built prototype performs well in the testing environment. Almost all measured parameters correspond to the simulation results. Only the power losses on the first inductor of the output filter need further investigation. The efficiencies stated in Table 2 are also promising for the prototype and simple hard switching full-bridge topology. Furthermore, the applied RST-controller in the simulation is showing results matching the requirements for fast scanning magnets.

## ACKNOWLEDGEMENTS

The authors would like to thank the team of the EMERGING APPLICATIONS LAB at MCI and furthermore MedAustron for giving us the opportunity to be part of their exciting environment and the unwavering support.

ISBN: 978-3-95450-214-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2021-TUPAB389



## REFERENCES

[1] R. Künzi, "Passive Power Filters", in *Proc. CAS - CERN Accelerator School: Power Converters*, Baden, Switzerland, May 2014, pp. 265-289. doi:10.5170/CERN-2015-003.265

[2] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high frequency gallium nitride based point of load converter", *IEEE Transactions on Power Electronics*, vol. 29, pp. 2008-2015, 2014. doi:10.1109/TPEL.2013.2266103

[3] E. Godoy and E. Ostertag, "RST-Controller Design: a rational teaching method based on two diophantine equations", *IFAC Proc. Volumes*, vol. 39, no. 6, pp. 541-546, 2006. doi:10.3182/20060621-3-ES-2905.00093

[4] K. Wellstead, "Robust Polynomial Controller Design", Ph.D. thesis, Department of Electrical Engineering and Electronics, Brunel University, Uxbridge, UK, 1991.

[5] IGOT60R070D1 600V CoolGaN™ enhancement-mode Power Transistor, www.infineon.com