

# DESIGN AND PERFORMANCE OF DIGITAL BPM PROCESSOR FOR DCLS AND SXFEL \*

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## Abstract

A digital BPM processor has been developed in SINAP, which can be used on the signal processing of both stripline BPM and cavity BPM. The processor is a standalone system and providing 4 channels 120MS/s, 16 bits ADC and powerful Virtex-5 FPGA. The processor has been applied on Dalian Coherent Light Source (DCLS) and Shanghai X-ray FEL (SXFEL). The processor specification and performance evaluations including lab and beam tests will be introduced.

## INTRODUCTION

Two FEL facilities, DCLS and SXFEL have been constructed and already under commission since last year in China. Both accelerators are constructed by Shanghai Instituted of Applied Physics (SINAP). The main BI instruments including stripline BPMs in LINAC and cavity BPMs in undulator section, the performance requirements are 10 $\mu$ m and 1 $\mu$ m at the beam charge of 0.5nC respectively.

BPM system can be decomposed into three parts: pickup, electronics, and cables that transferring signals between them. A wide variety types of BPM pickups have been designed to couple different types of accelerator beam signals. FEL is single pass electron beam accelerator. Stripline BPM(SBPM) is wide band pickup used in the LINAC, cavity BPM(CBPM) is narrow band pickup used in undulator section for its high resolution. Figure 1 is the corresponding BPM signal.

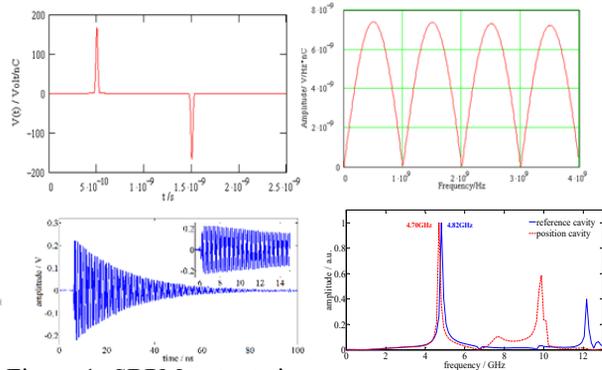


Figure 1: SBPM output signal (top left) and the spectrum (top right), CBPM output signal (bottom left) and the spectrum (bottom right)

Electronics is used to process the pickup output signal to get position information and supply it to high-level users through Ethernet, it mainly composed of RF signal conditioning, digitizer, digital signal processing, data

acquisition and transmission. Figure 2 is the block diagram of BPM system.

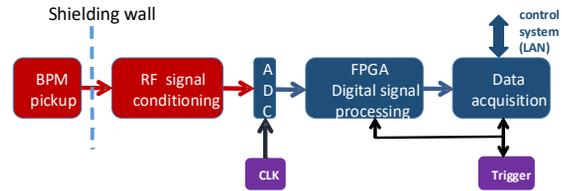


Figure 2: BPM system block diagram.

The frequency range of the SBPM output signal is too wide to process, BPM electronics choose part of it to calculate the position. Some processors integrate the function with digitizer and acquisition (DAQ) to make a standalone instrument.

The CBPM resonant frequency of DCLS and SXFEL is about 4.7GHz at C band. It's much higher than the bandwidth of most ADC, and should be down converted to intermediate frequency(IF) before digitized. Routinely this function is implemented by coaxial RF devices which is independent of DAQ system.

A prototype of standalone BPM processor has been designed at 2012, which can be used to process the BPM signal on the SSRF synchrotron storage ring[1][2]. Based on previous work, a new single pass processor is designed to handle the signal processing of both SBPM raw signal and CBPM intermediate frequency signal.

## PROCESSOR OVERVIEW

The processor can be decomposed into following functions: RF signal conditioning, analogue to digital ADC, digital signal processing, data transmission and control. All functions are integrated into a standalone instrument. RF conditioning and ADC locate on RF board, others on digital carrier board. Figure 3 is the architecture of the processor.

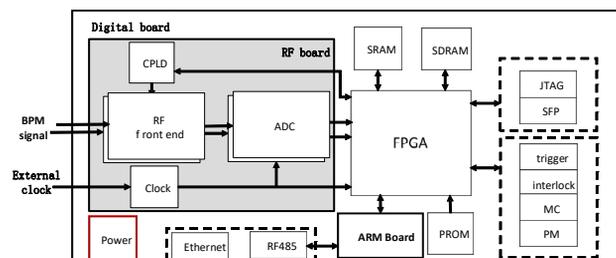


Figure 3: Processor architecture.

RF conditioning includes SAW band-pass filters, which central frequency is 500MHz and -3dB bandwidth is 12MHz. The IF signals from CBPM locate at this frequency range too. The analogue signals are control at an appropriate level with attenuators and amplifiers to fit ADC's best performance. Signals after conditioning are

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sampled with ADCs (16bits, 120MHz) by means of undersampling theory. The digitized signal is fed into FPGA (Xilinx xc5vfx70t) for signal processing. The system is controlled by an embedded system on ARM, which running EPICS IOC to transfer data and command.

### HARDWARE DESIGN

Four channels are included on the RF board (only three of them will be used on CBPM signal processing). Figure 4 is the RF signal processing chain. The attenuation control value can be set between 0~31dB. The ADC chip type is 16 bits AD9265, which maximum sample rate is 125MHz and bandwidth is 0~650MHz. ADC clock source can be selected between on board oscillator (117.2799MHz) or external input clock. Figure 5 is the spectrum of sampled signal from RF board.

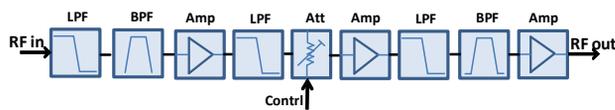


Figure 4: RF signal processing chain.

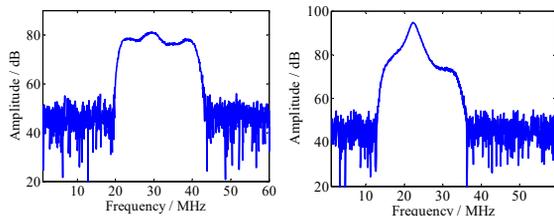


Figure 5: Spectrum of signal from RF board of SBPM (left) and CBPM (right).

Carrier board is based on a Xilinx FPGA XC5V5X50T and ARM chip Freescale iMX6q. The digital data and clock source from RF board is connected into the FPGA. The FPGA handles the data processing and communication with peripheral components, including SRAM, SDRAM, ARM, and CPLD on RF board. FPGA send RF configure command to CPLD through SPI bus. The interface between FPGA and ARM is a two lane PCIE. Figure 6 is the board hardware.



Figure 6: RF board (left) and Digital board (right) hardware.

### FIRMWARE AND SOFTWARE DESIGN

The firmware in FPGA implements two main functions. One is the interface logic, including the SRAM and SDRAM controller, PCIE, SPI, ADCs, clock and trigger.

The other is signal related algorithms, including beam arrive judgement, data capture FIFO and data processing. Figure 7 is the block diagram of the firmware design.

The firmware will generate an internal trigger signal when beam arrives, and capture 1024 points data before and after the trigger. Also the trigger signal can be chosen between internal and external source.

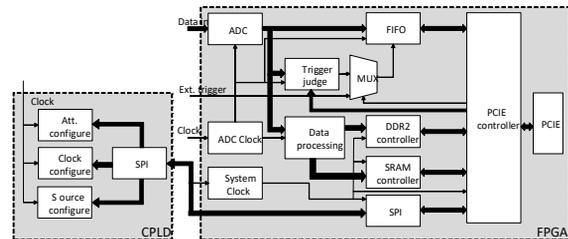


Figure 7: Firmware diagram.

ARM runs arm-LINUX operation system, and integrated EPICS IOC. Beam position calculation is implemented at IOC level for the low repetition rate. The IOC implements following functions: system configurations, including trigger source, clock source, trigger threshold value, attenuation value; two signal amplitude and phase calculation algorithms FFT and Hilbert are implemented for user selection; position calculation for different BPM. Figure 8 is the software functions. Figure 9 is the processor picture and EDM control panel.

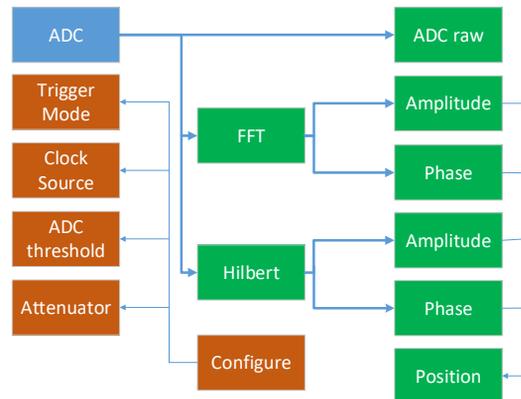


Figure 8: Software functions.

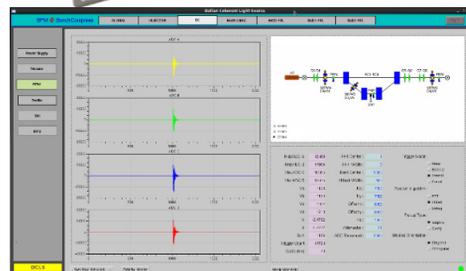


Figure 9: Processor and EDM user panel.

## PERFORMANCE EVALUATION

The processor performance has been evaluated in lab. The ADC noise RMS is about 6 when attenuation is larger than 16dB. The ADC SNR contour figure show that the ENOB is about 10bits. Figure 10 is the noise level evaluation results and SNR contour picture.

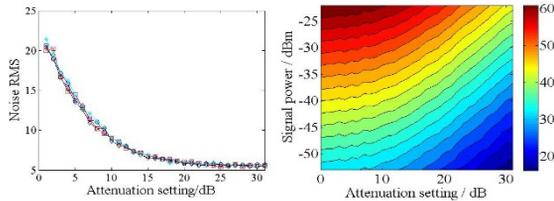


Figure 10: Noise level(left) and SNR contour.

On-line resolution tests have been carried out by connecting two split SBPM A/C and CBPM Y/Ref signal to processor four inputs. The resolution value is  $k \cdot \text{std}(u1 - u2) / \sqrt{2}$ ,  $k$  is the calibration factor of SBPM and CBPM,  $u1$  and  $u2$  are the two calculated normalized position value.

The bunch charge is about 500pC, attenuator is configured to 16dB. Results show that the processor relative resolution is better than  $10^{-3}$  when ignoring the  $k$  factor. The  $k$  factor of SBPM and CBPM is 7.59mm and 300um respectively, and the calculated resolution of SBPM and CBPM is  $4\mu\text{m}$  and  $0.4\mu\text{m}$  as show in Figure 11.

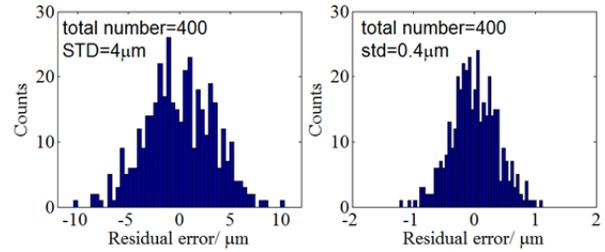


Figure 11: Resolution test results of SBPM (left) and CBPM (right).

## CONCLUSIONS

The processor meets the requirements of DCLS and SXFEL and applied on the projects successfully. Further developments and optimizations will be carried out to make it fit the processing of higher bunch repetition rate and synchrotron facility.

## REFERENCES

- [1] L.W.Lai, Y.B.Leng, Y.B.Yan, Z.C.Chen, "An Intelligent Trigger Abnormal Beam Operation Monitoring Processor at the SSRF", MOPTY020, IPAC2015, Richmond, USA(2015), pp.978-980.
- [2] L.W.Lai, Y.B.Leng, Y.B.Yan, W.M.Zhou, F.Z.Chen, J.Chen, Z.C.Chen, "Batch Applications of Digital BPM Processors from the SINAP", WEPG17, IBIC2016, Barcelona, Spain(2016), pp.658-660.