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# REAL-TIME CONTROL SYSTEM UPGRADE OF THE CERN LINAC4 PRE-CHOPPER

M. Niccolini*, T. Gharsa, F. Vaga, N. Magnin, C. Boucly, CERN, Geneva, Switzerland



*Abstract*

The CERN Linac4 pre-chopper, installed right after the H- ion source in the Low Energy Beam Transport (LEBT) section, plays a crucial role in providing the 45 keV H- beam to the first accelerating structure, the Radio Frequency Quadrupole (RFQ). By applying a pulsed electric field of -20 kV, the pre-chopper deflects the beam when not required and sharps its head and tail in order to remove the long rise time of the source and avoid transmission losses. The existing pre-chopper controller was implemented in 2015 using National Instruments (NI) LabVIEW and PXIe hardware, relying on their proprietary Real-Time (RT) operating system (Phar Lap) and a secondary Linux Front-End Computer (FEC) for the integration in the CERN control system. Phar Lap is EOL since 2025 and will be discontinued during the upcoming Long Shutdown 3 (LS3). This paper presents an upgrade of the control system, aimed at replacing the LabVIEW-RT control layer with standard CERN solutions, leveraging the new Debian-based Linux RT OS, Front-End Computer Operating System (FECOS), and consolidating all functionalities into a single computer. The goal was achieved using the CERN Front-End Software Architecture (FESA) 3 framework and C++ libraries to interface with the NI hardware via NI Linux drivers deployed on FECOS. A new PyQt-based graphical user interface will be developed to ease system monitoring and operation. Installation of the upgraded system is expected for LS3, using a custom PXIe crate and CPU from CERN instead of NI solutions.

## INTRODUCTION

The pre-chopper is located in the Linac4 [1] LEBT and deflects the beam away from the RFQ input aperture when it is not required. It serves to reduce the beam start-up time from the H- source, to shorten its pulse length, and to stop the beam due to machine interlocks. The beam is chopped by applying -20 kV to a plate in vacuum, which is switched to 0 V when the beam should pass. Figure 1 shows the position of the system in the accelerator. The beam is chopped (-20 kV applied) before the H- ion source is started by receiving a first trigger signal (Pre-chop1, see Fig. 2). To start to deliver the beam to the RFQ, the voltage is switched to 0 V (Pre-chop2). Once the PSB (Proton Synchroton Booster, the next accelerator in the chain after LINAC4) has finished the injection sequence, which is of variable length depending on the type of beam produced, the pre-chopper deflects the beam again (Pre-chop3). Once the ion source stops, the pre-chopper plate returns to 0 V (Pre-chop4). The pre-chopper has also the role of deflecting the beam if it is not required due to an interlock condition provided by the Beam Interlock System (BIS) [2]. Since the application of -20 kV onto a deflection plate is inherently not fail-safe, the pre-chopper must be used in conjunction with additional beam inhibiting devices, managed at the level of BIS.

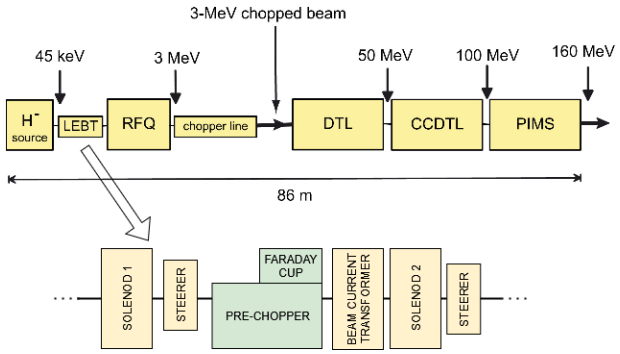


Figure 1: Schematic layout of the Linac4 accelerator. The LEBT section is shown in an exploded view, highlighting the the pre-chopper position.

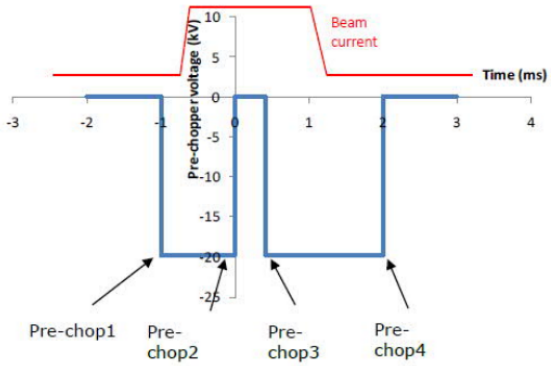


Figure 2: Pre-chopper high voltage pulse timing sequence.

### *Motivation for the Upgrade*

The eradication of the LabVIEW RT is motivated by the obsolescence of Phar Lap, no longer supported by NI since 2025 [3] and of the NI library used with SILECS (Software Infrastructure for Low-level Equipment Controller, formerly known as IEPLC [4]) to interact with the CERN control system stack. A control solution based on FESA 3 [5] and LabVIEW FPGA is proposed as an upgrade that simplifies the integration in the CERN control system architecture.

## CONTROL SYSTEM LAYOUT

### *The Current Control Layout*

The pre-chopper control functionalities, depicted in Fig. 3, are deployed on an NI PXIe controller (NI PXIe-8100) as-

* marco.niccolini@cern.ch

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sociated with a NI Multifunction Reconfigurable I/O Module (RIO) FPGA board (NI PXI-7851R). Most of the pre-chopper control logic has been implemented at the level of the RIO device using LabVIEW FPGA; on the PXIe controller, a LabVIEW RT program manages the state of the system and of the High-Voltage (HV) power-supply. To interface the NI PXIe crate with the CERN Control system [6], a second computer runs a FESA process, that communicates with the LabVIEW RT through SILECS. This Kontron computer also hosts the General Machine Timing (GMT) [7] receiver, needed to trigger the HV pulse sequence, and a Spectrum M2i.3013 digitizer to monitor the waveform of the pulse, using the IPOC software [8]. A LabVIEW GUI is available as expert tool for equipment diagnostic and system test.

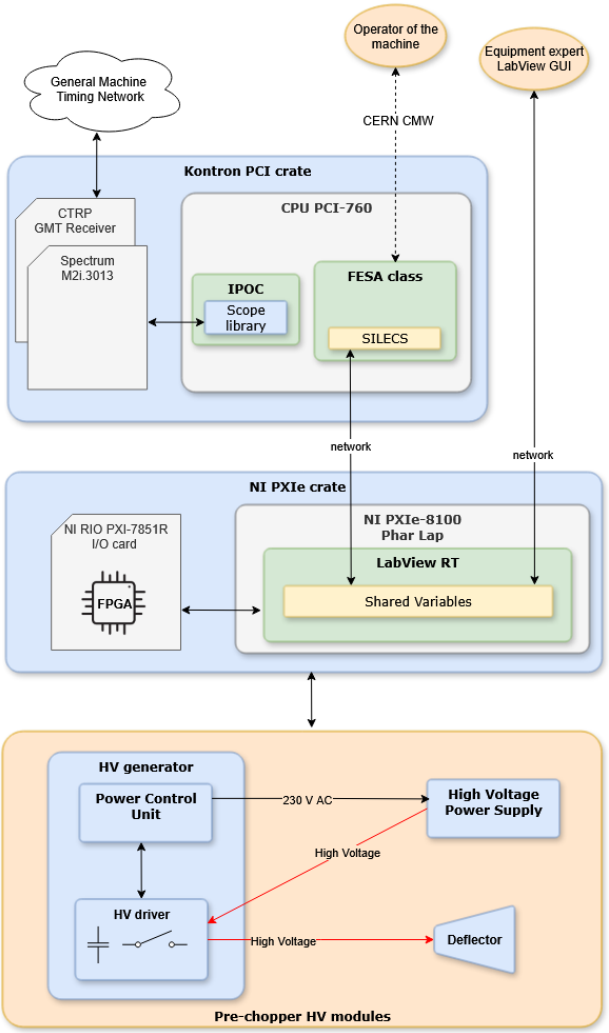


Figure 3: Simplified synoptic of the current system architecture.

## *The Upgraded Control Layout*

Figure 4 illustrates the new system architecture.

The upgraded control system replaces the previous dual-computer architecture (comprising a Kontron PCI computer and a NI PXIe crate) with a single FEC. A new FESA class running on this FEC implements the control functionalities previously done in LabVIEW RT. It interfaces directly with the NI RIO FPGA, eliminating the need for the SILECS communication layer. The GMT receiver and the digitizer used for IPOC waveform acquisition have also been integrated into the new FEC. All hardware and software dependencies are now combined into a single platform. The following sections describe the migration from the legacy NI-based solution, detailing the hardware and software components introduced or modified. The upgraded system has been deployed on a dedicated test bench at CERN, where high-voltage discharge pulses can be triggered to validate system performance ahead of installation during LS3.

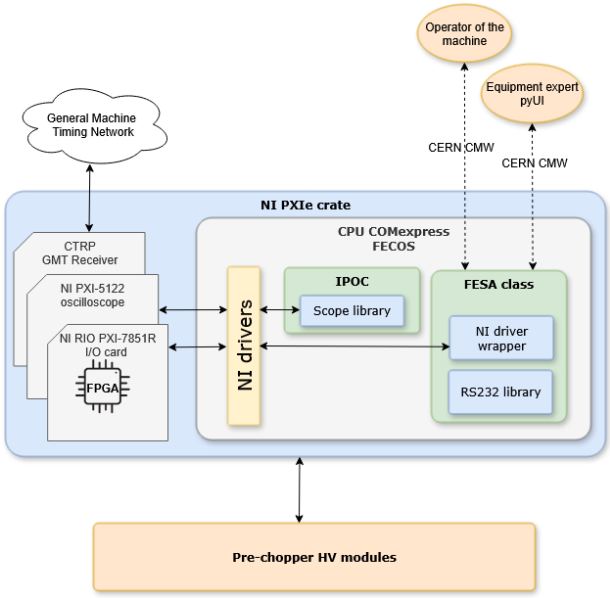


Figure 4: Synoptic view of the new system architecture. The HV modules for the pre-chopper are not shown, as they are identical to those presented in Fig. 3.

## *The Test-Bench*

To ensure the upgraded system meets operational requirements, a test bench replicating the core components of the Linac4 pre-chopper installation has been assembled. It includes the HV driver, the Heinzinger HV power supply, and the Power Control Unit (PCU), allowing the system to be pulsed and monitored in a safe environment.

A capacitive dummy load replaces the actual deflector, enabling testing of the HV pulse generation. The HV driver features a capacitor bank charged by the HV power supply and a BEHLKE switch that applies the -20 kV voltage to the dummy load. Voltage measurements are taken using three HV dividers: one across the capacitor bank and two across the dummy load, providing the NI RIO card with complementary resolution for low-voltage and high-voltage regions.

The HV power supply is controlled via RS232 by the PXIe controller and the PCU manages the interface between

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the FPGA and the BIS, as well as the connection to the HV driver and the control of the 230 V mains. This setup provides a platform for validating the control logic, timing synchronization, and safety mechanisms prior to operational deployment.

## CONTROL HARDWARE

### *PXIe Crate and Controller*

The system uses a commercial NI PXIe-1082 chassis, equipped with a custom PXIe controller developed within the CERN SAMbuCa project [9], that replaces the discontinued NI PXIe-8100 and provides enough RAM for the network boot of FECOS. This new controller is based on a COM Express module [10], featuring an Intel® Core™ i5-11500HE @ 2.60 GHz and 15.7 GB of RAM. This custom solution ensures compatibility with CERN's infrastructure and leverages developments from other projects, contributing to a reduction in development and integration costs.

### *National Instruments Cards*

The PXIe crate hosts two NI cards:

- NI RIO FPGA (PXI-7851R): A Virtex-5 LX30-based multifunction reconfigurable I/O module. It handles the core logic of the pre-chopper, including pulse shape surveillance, interlocks handling in interaction with the BIS, and the control of HV driver switch command. It is the same card used in the previous layout and the gateware, developed using the NI LabVIEW FPGA module, remains unchanged to mitigate redevelopment effort.
- NI Digitizer (PXI-5122): A 100 MHz bandwidth oscilloscope used to acquire the full high-voltage pulse waveform for monitoring and logging purposes.

### *Central Timing Receiver*

The timing of the deflector pulses is synchronized with the CERN accelerator complex via the GMT network. A Timing Receiver card is installed on a PXI-compatible carrier [11], enabling the triggering of the pulse sequence at each machine cycle.

## CONTROL SOFTWARE

### *FECOS*

The upgraded system runs on FECOS, CERN's standard front-end operating system based on Debian 12, with a transition to Debian 13 expected soon. FECOS is fully integrated into CERN's infrastructure, supporting network boot, centralized configuration via the CCS (Controls Configuration Service, [12]), shared file system access, and centralized support. This setup allows the FESA class to run directly on the PXIe crate, eliminating the need for the secondary FEC previously required for signal acquisition and the integration in the general CERN control system.

### *NI Linux Drivers*

NI provides Linux drivers for its hardware via Dynamic Kernel Module Support (DKMS) packages, which compile kernel modules dynamically during installation or upon kernel upgrades, and store the resulting binaries on a local disk. However, CERN's front-end computers are diskless and lack, on purpose, toolchains for compilation. To address this, the FECOS team repackages the NI drivers in binary format for internal distribution. These drivers are loaded during the FEC boot sequence, from a Network File System (NFS).

### *NI RIO Wrapper Library*

To facilitate integration with the FESA framework, a custom wrapper library was developed around the NI-provided C APIs. This wrapper:

- Loads the FPGA bitstream.
- Simplifies access to the memory-mapped registers, e.g. implementing register value conversions.
- Implements a singleton pattern to manage shared resources via a global access point.

The library development builds upon previous experience integrating NI gateware into a FESA class [13].

### *High Voltage Power Supply Communication*

A dedicated serial RS232 communication library was developed to interface with the Heinzinger High Voltage power supply. It enables parameter configuration and runtime monitoring of current and voltage, ensuring exclusive access to the serial port used.

### *Real-Time Software*

The RT logic, previously implemented in LabVIEW RT, has been re-engineered in C++ using the FESA framework, CERN's standard for control software development. The FESA class manages system operation, interlock statuses, and power supply control. It implements a State Control and Surveillance System (SCSS) by providing interfaces for both operators and experts to:

- Control system state (ON/OFF).
- Monitor status and alarms.
- Configure operational/expert parameters.

It also retrieves waveform data from the FPGA around the transition point of each pulse, allowing the expert to monitor critical phases of the cycle. All software runs on the FEC using the libraries described above.

### *Internal-Post Operation Check System (IPOC)*

Leveraging the digitizer card installed in the PXIe chassis, the system acquires the full HV pulse waveform after each operation. This data provides the expert with a view of the pulse shape, and it is available for logging, troubleshooting and automated analysis. This functionality is based on a standard building block used across multiple beam transfer systems within the accelerator complex, the IPOC.

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## NEXT STEPS AND FUTURE WORKS

Enhancements are planned to further improve the system and prepare it for long-term operational deployment:

- Graphical User Interface: a PyQt-based graphical user interface will be developed to provide expert-level control and monitoring capabilities and replace the existing LabVIEW GUI. This interface will use the upcoming CERN PyUI framework based on PyQT, ensuring consistency across systems.
- Gateware upgrade: future revisions of the FPGA gateware will improve the handling of the Internal Post Operation Check (IPOC) trigger mechanism. Currently, waveform acquisition is initiated on every machine cycle, regardless of the equipment's operational state. The planned upgrade will ensure that acquisition is performed only during user-enabled cycles.
- Configure an IPOC analyser for automated waveform checking and interlocking of the system based on results of the analysis.
- High Availability PXIe Chassis: the system will be migrated to a CERN-developed PXIe High Availability chassis, based on the NI 1082 backplane. This chassis features redundant power supplies and fan trays, along with a monitoring card for diagnostics and remote management. This hardware platform is shared with the SAMbuCa project, promoting standardization and maintainability.
- Deployment to similar systems: the architecture developed for the Linac4 pre-chopper is applicable to other LabVIEW RT system with similar HW. In particular, the electrostatic deflectors used in the beam transfer lines to the Extra Low Energy Antiproton ring (ELENA) share a comparable layout. The upgraded control solution could be extended to these systems, enabling the replacement of the existing LabVIEW RT implementation with a standardized and maintainable CERN-based approach.

## CONCLUSIONS

The upgraded control system has been installed in a high-voltage test cage at the CERN test facility, where it has been operating continuously for the past few days. The equipment is synchronized with the real machine timing and has successfully pulsed at reduced voltage levels, validating the control logic and timing integration.

Figure 5 shows a representative waveform acquired during operation of the test-bench at 15 kV with the dummy load. The FEC has maintained continuous operation, with NI hardware accessed on every cycle, and no instabilities have been observed.

These first results validates the upgraded control and with few added features it will be ready for deployment during LS3.

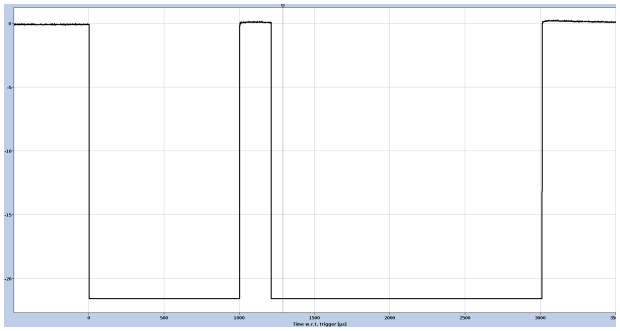

Figure 5: Waveform of the complete pulse sequence acquired on the test bench. Voltage values are uncalibrated.

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