Distributed I/O Tier as a Reference Platform

for Harnessing System-On-Chips in CERN's Control System:

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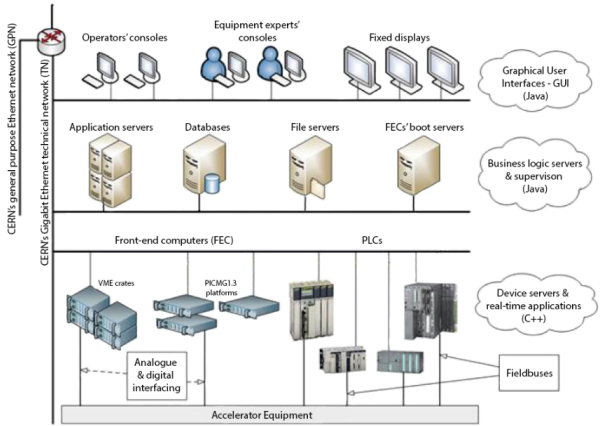
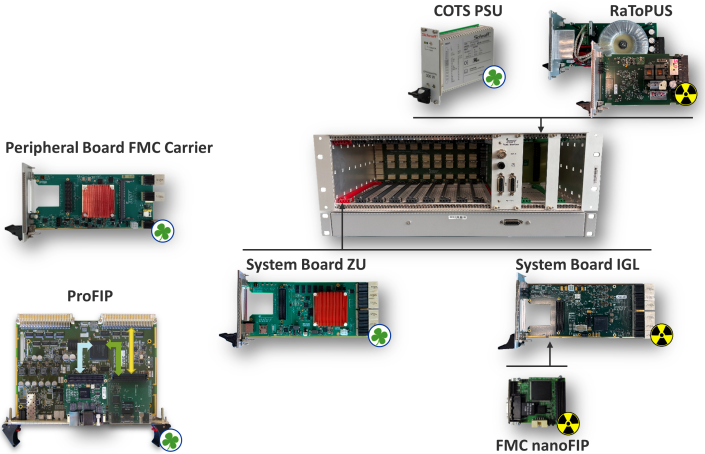
Introduction

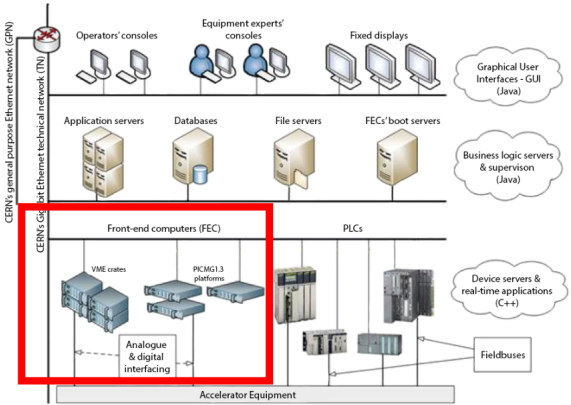
CERN's Control System Architecture



DI/OT Hardware Kit



Where DI/OT fits



What it is provided with DI/OT platform

- Modular and scalable build system (AMD Xilinx SoCs + FPGAs)
- Reference gateware design
- Reference patch set for the bootloaders
- Reliable Booting mechanism
- Basic monitoring services

Build system

Features

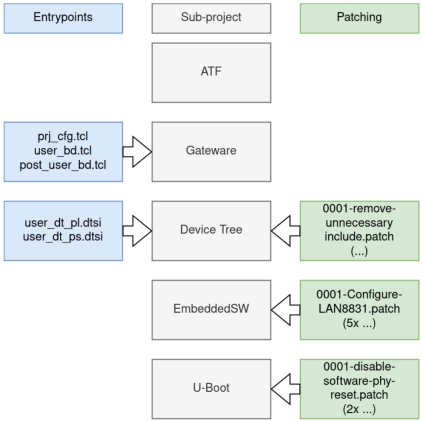
- A complete build system for AMD Xilinx ZynqMP SoC
  - Generates BOOT.BIN & binary components
- Leverages standard wide-spread tools
  - Base on TCL scripts(Python), bash and GNU make
- Incremental compilation in all stages
  - Reports outdated builds

```
mkdir -v -p build_dir/diot_v4/sentinels/projects/diot_v4/tcl b
iot_v4/tcl build_dir/diot_v4/sentinels/projects/diot_v4/tcl
touch build_dir/diot_v4/sentinels/projects/diot_v4/tcl/post_us
ls/projects/diot_v4/tcl/create_bd.tcl.sentinel build_dir/diot_
=== DI/OT TAMPER WARNING (project gateware) ===
The following files were changed:
- gateware/projects/diot_v3/constraints/fmc.xdc
- gateware/projects/diot_v3/src/emio_ctrl.vhd
- gateware/projects/diot_v3/tcl/platform_addressing.tcl
- gateware/projects/golden_v4/tcl/ps_cfg.tcl
=== User is at its own risk. ===

****** Vivado v2024.2 (64-bit)
  **** SW Build 5239630 on Fri Nov 08 22:34:34 MST 2024
  **** IP Build 5239520 on Sun Nov 10 16:12:51 MST 2024
```

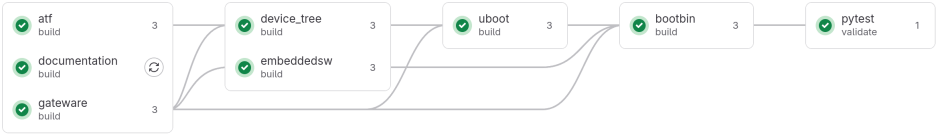
Features

- Easy to expand
  - Implement new builds (RPUs)
  - Easy to add user patches



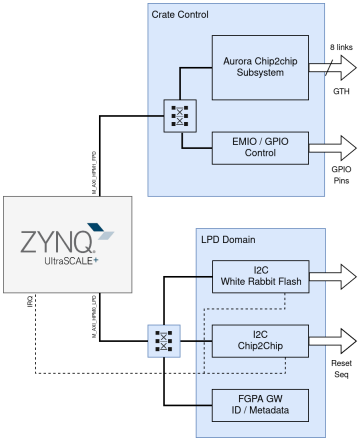
Features

- User friendly with CI/CD
  - Exploits CI4FPGA infrastructure
- Hardware-in-the-loop through pytest



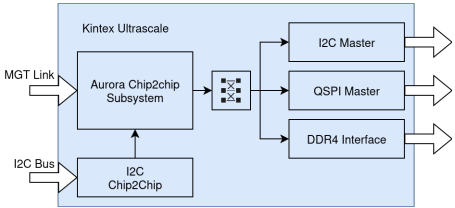
Reference design

DI/OT Reference Design (SB)



- PS default configuration
- Aurora + Chip-to-Chip (C2C)
- AXI I2C PL Master
- PL+PS GPIO interface
- Facilitate Device Tree integration
- Reprogramming interface for peripheral boards

DI/OT Reference Design (PB)

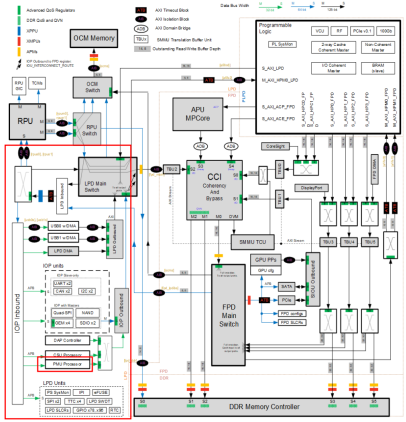


- Aurora + Chip-to-Chip (C2C)
- AXI I2C PL Master
- AXI I2C QSPI
- AXI DDR SO-DIMM (8GB)
- Device Tree overlays for peripheral boards

Remote console

Remote console

- PMU: MicroBlaze 32b CPU
- Full access to the peripherals
- Software-controlled UART0 <=> UART1 loopback
- Dual queues in the Ethernet controller with packet filter

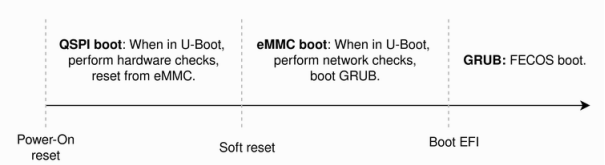


Remote console

- Minimalistic IPMI/RMCP v 1.5 stack (port 623)
- Minimalistic BOOTP/ARP daemons
- IPMI v 1.5 remote reset + power cycle (HW-specific)
- IPMI v 1.5 Serial-on-LAN (SoL) console
- Password authentication with MD5 hashing
- Password update over IPMI/RMCP
- No more features due to memory limitations

Reliable booting & Monitoring

Reliable booting



- Boot process split into two stages:
  - QSPI golden boot
  - eMMC user boot
- QSPI boot image ensures recovery from corruption
- eMMC BOOT.BIN includes custom FPGA bitstreams
- Both images are able to boot FECOS from the network
- Prevent failures during boot, upgrades, or runtime
  - Limited by SoC ROM and FSBL vulnerabilities

Monitoring

- HWMON Framework and collectd
- Cosmos Framework from CERN

Conclusions & Outlook

- DI/OT: reference SoC platform for CERN controls
- Build system: CI-driven, automated DT generation, custom IP integration
- Reliable booting for FECOS and suported monitoring with HWMON, collectd and COSMOS
- Outlook:
  - Remote reset & Serial-over-LAN via lightweight IPMI/RMCP in PMUFW
  - Remote reprogramming: secure FPGA/firmware updates over network
  - Enhanced monitoring tooling with new features & updates


CERN