PandABox II: A Collaborative Platform Designed for Future Upgrades

Y-M. Abiven on behalf of the collaboration team
SOLEIL, DIAMOND, ALBA, DESY and MAXIV

SOLEIL II
La science éclaire l'avenir
Science lights up the future

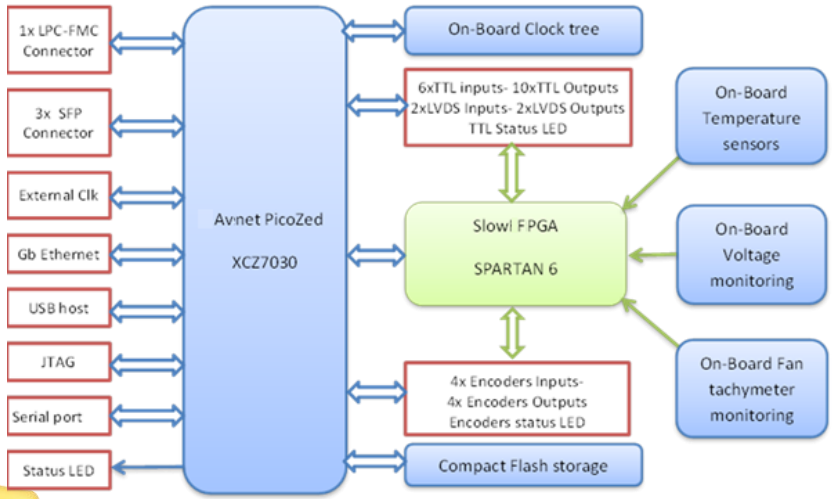
Outline

- PandABox II collaboration
- PandABox status
  - firmware, software and applications
- PandABox II Designs status
- Summary and next steps

PandABox II collaboration

SOLEIL II
La science éclaire l'avenir
Science lights up the future

PandABox collaboration



- PandABox
  - Developed by SOLEIL and DIAMOND 10 years ago
  - Open Hardware and Open Source Platform, available on CERN OHWR repository and Github repository.
- PandABox around the world
  - Europe : SOLEIL, DIAMOND, MAX IV, and DESY,
  - America : NSLS-II,
  - Asia: HEPS,
  - Middle East : SESAME.
- Collaboration extension with SOLEIL, DIAMOND, MAX IV, ALBA, and DESY
  - Following discussion in LEAPS INNOV project[1]
  - Objectives to maintain a state-of-the-art platform
  - Enhancing features for synchronization requirements in light source experiments
  - Sharing experience with developers community

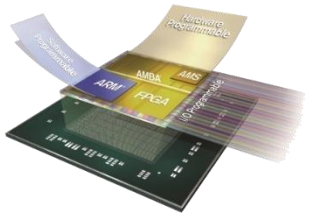
[1] https://www.leaps-innov.eu/

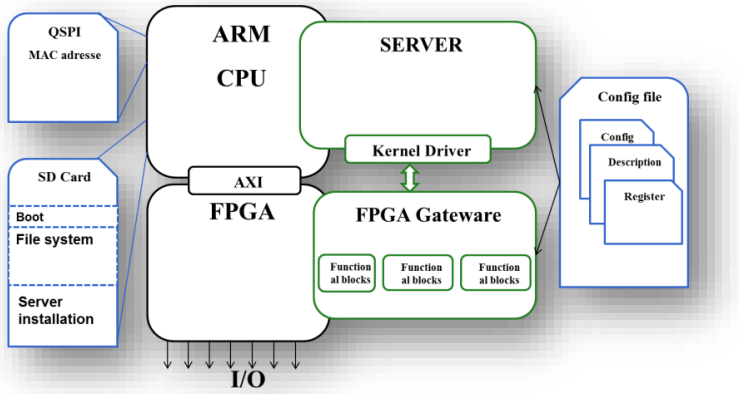
PandABox status

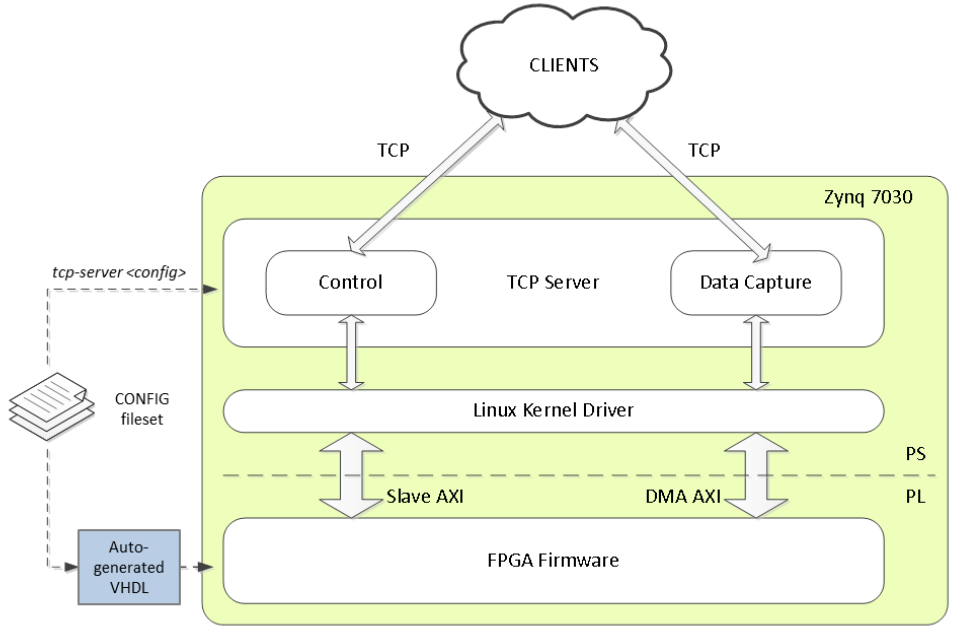
SOLEIL II
La science éclaire l'avenir
Science lights up the future

PandABox: Firmware & Software architecture

- Flexible and configurable architecture







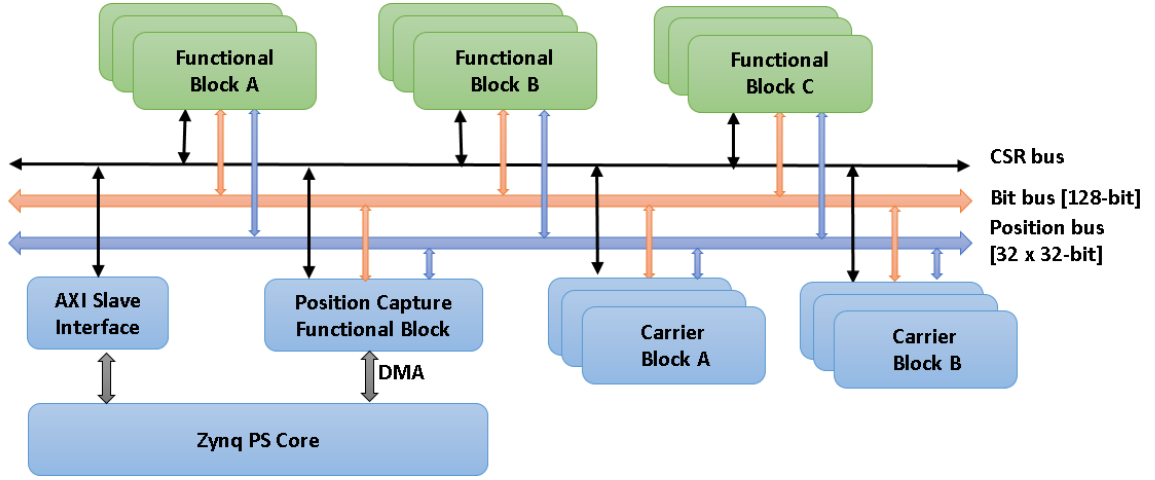
  - FPGA firmware layer
    - Structured into numerous Functional Blocks (FBs)
  - TCP-Server layer
    - **Two socket endpoints** to connect to clients (EPICS, TANGO, etc.)
      - configuration **control** (control & status register)
      - streamed data capture (interface with DMA engines for synchronous R/W)

⇨ 2 layers **tightly coupled** through **a common set of configuration files** (FB's I/O ports, configuration registers, and descriptions)

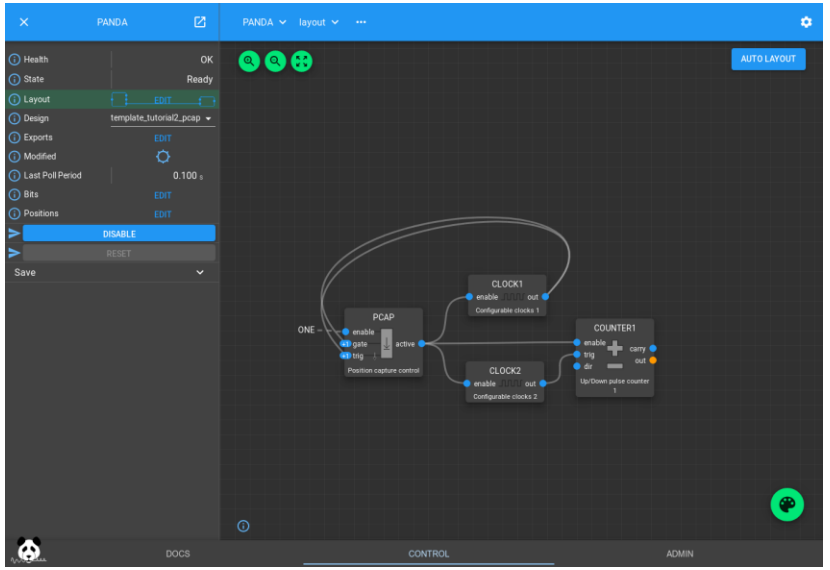
⇨ Allowing to **design and compile** a custom set of **FBs** into the **firmware** with **access from the TCP Server**

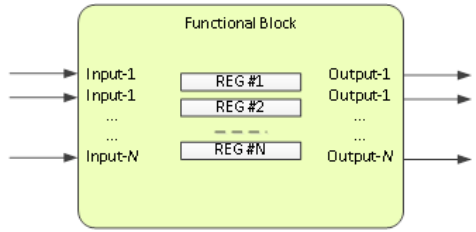
- Fully re-wirable (at run-time) architecture

- Physical and logic interface connected together by:
  - 128-bit Bit-bus and Position-bus
- Logic block functionalities
  - BITS - Soft inputs and constant bits
  - CALC - Position Calc
  - CLOCK - Configurable clock
  - COUNTER - Up/Down pulse counter
  - DIV - Pulse divider
  - FILTER - Filter
  - FMC_ACQ427 - FMC ACQ427 Module
  - INENC - Input encoder
  - LUT - 5 Input lookup table
  - LVDSIN - LVDS Input
  - LVDSOUT - LVDS Output
  - OUTENC - Output encoder
  - SFP_DLS_EVENTR - SFP Event Receiver Module
  - PCAP - Position Capture
  - PCOMP - Position Compare
  - SEQ - Sequencer
  - etc.
- Custom Functional Blocks can be added
  - Each FB contains:
    - Discrete bit-type input and output ports
    - 32-bits wide position-type input and output ports
    - Configuration and status registers



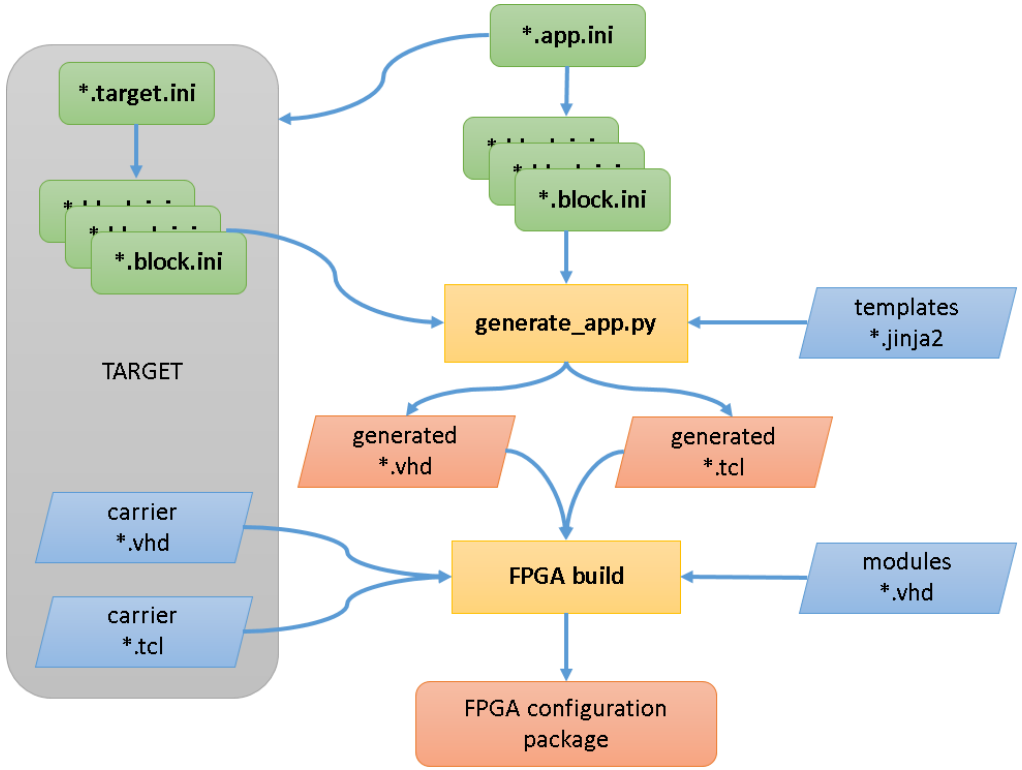
https://pandablocks-fpga.readthedocs.io/en/latest/blocks.html





FPGA auto-generation framework

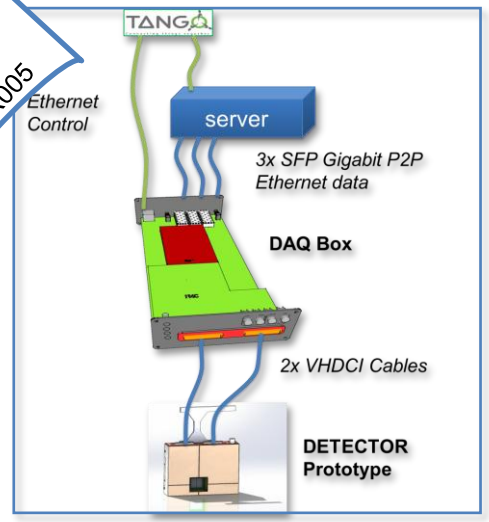
- Goals
  - Simplify inclusion of user-generated functional blocks
  - Implement arbitrary combinations of ‘soft’ and hardware blocks
  - Simplify targeting other Zynq-based hardware platforms
- Implementation
  - Set of text-based “ini” files
  - “app.ini” – set of ‘soft’ function blocks in design
  - “target.ini” – set of ‘carrier blocks’ available on the hardware
  - “block.ini” – defines register interface for each block + other information, e.g., IP, constraints required
- HDL wrappers and register interfaces for each block generated from templates using Python and jinja2 template engine
- Top-level Makefile drives the build flow



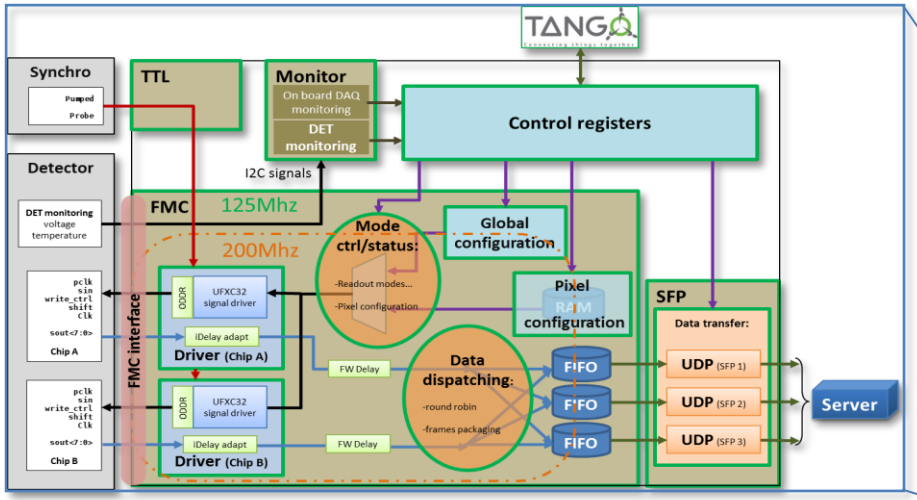
Jinja

Capabilities for custom application

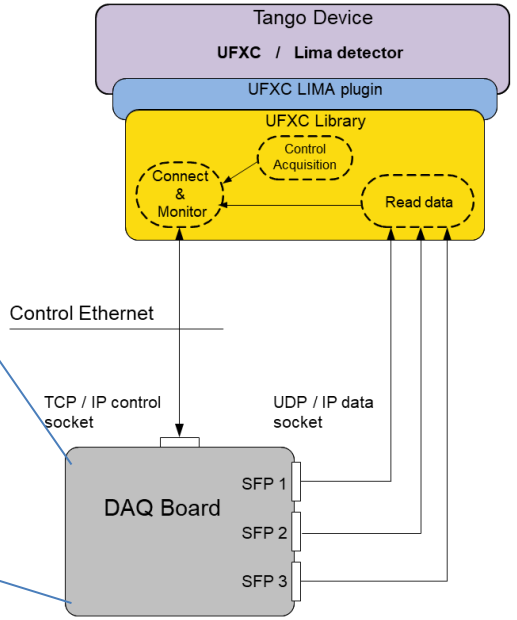
G.Thibaux et al,
doi:10.18429/JACoW-ICALEPCS2019- MOMPR005



DaQ architecture of a UFX photon-counting detector



DAQ Firmware Architecture

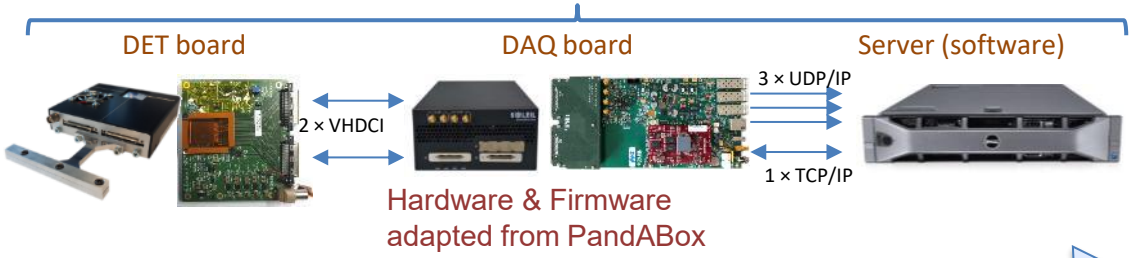


- PandABlocks
  - Detector settings and the control of the acquisition are controlled by the Tango software over the TCP Ethernet network
- Specific data streaming to retrieves the detector data chunks, build data packets and to dispatch them, in a round robin manner
  - UDP/IP protocol with point-to-point Ethernet links.
  - 3 SFP UDP block based one an OpenCores UDP IP Stack[1], each sending Gigabit Ethernet UDP/IP frames
  - FMC block, a 200 MHz clock domain has been used to comply with the image readout frame rate

[1]OpenCores UDP IP Stack, https://opencores.org/projects/udp_ip_stack

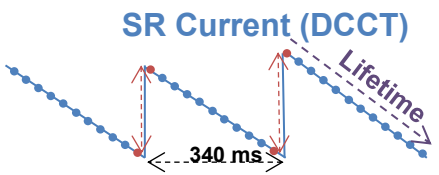
Applications based on PandBlocks

- **UFX detector DAQ interface**



Hardware & Firmware adapted from PandABox

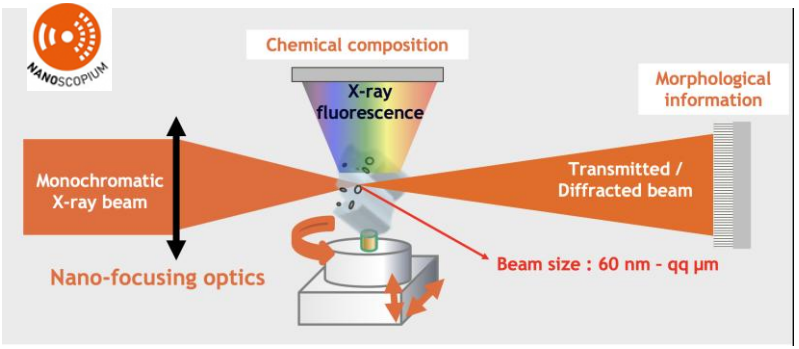
- **CIEL (Current Injection Efficiency and Lifetime) :**
  - New acquisition system for the DCCT



DMM NI PXI 4071

FMC 24 bits ADC

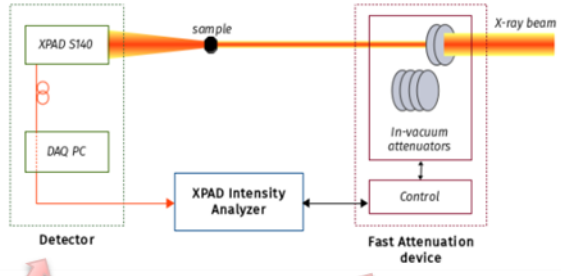
- **Continuous scan applications (Flyscan)**



- Beamline DAQ systems upgrade:
  - QEXAFS monochromator position and ionization chamber captures
  - Strain gauge measurement for the fatigue test machine
  - Nanoprobe interferometer position captures
  - …

- **FastATT XPAD: Upgrade of the real-time control system for the Fast beam-ATTenuation with an XPAD detector**

Global architecture of the XPAD controlled beam-attenuation system



cyclic estimation of photon flux

continuously adapts beam attenuation

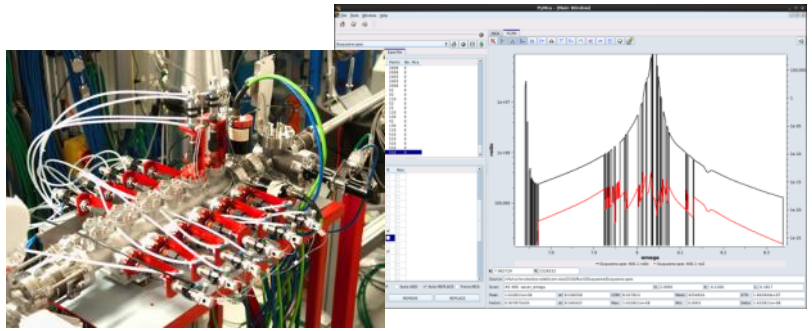


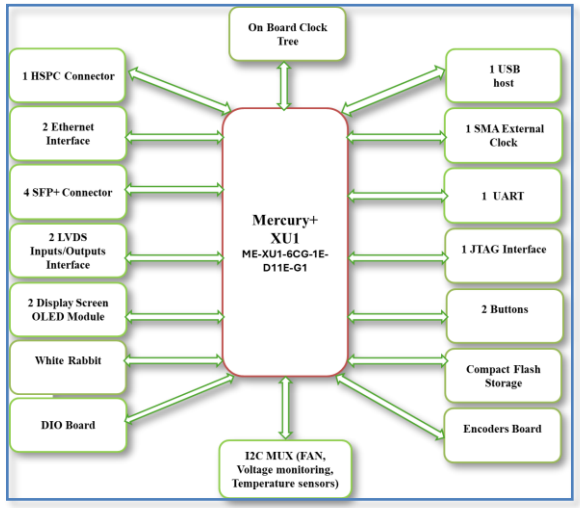
Fig.: attenuation system installed on the SixS beamline at SOLEIL

SOLEIL II
La science éclaire l'avenir
Science lights up the future

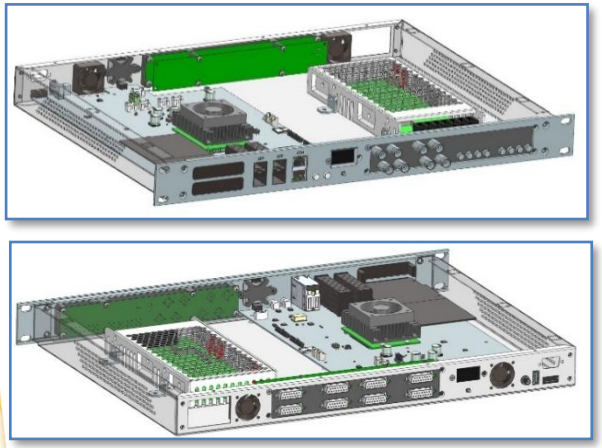
PandABox II Designs status

SOLEIL II
La science éclaire l'avenir
Science lights up the future

PandABox II Hardware status



Functional chart of the PandABox II



Front and Back panel view or the 19" rack design by DESY

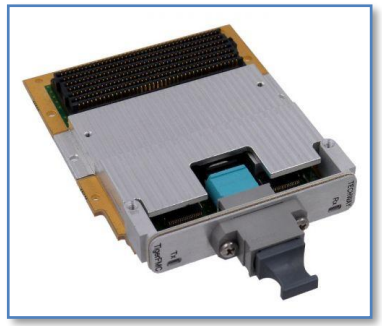
- Hardware changed on the PandABox II
  - Processor based on Enclustra Mercury+ XU1
    - ME-XU1-6CG-1E-D11E-G1
  - 2X Ethernet RJ45 port
    - For control
    - For administration purposes or Ethercat
  - 16 MGTs available
    - 4 on the carrier board
    - 12 routed on the High-Speed Serial Pin Connector (HSPC) of the FMC
  - 1 LCD display for board status monitoring
  - 16 Multi-Channel TTL and LVDS I/Os for synchronous triggering and clocking signals via BNC and LEMO connectors.
  - Fine delay (10 ps resolution) on selected digital outputs
  - 8x bi-directional encoder channels
- Status
  - Carrier and DIO boards prototypes are under unit tests
  - Test Firmware provide by Diamond to test the I/O

Carrier board prototype design by SOLEIL; populated with enclustra SOM and D-tacq ACQ427

Front panel I/O Board design by Alba

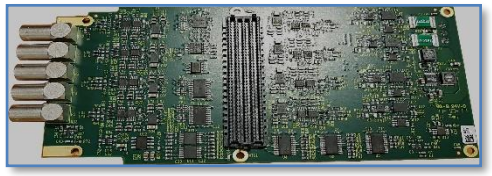
Back panel I/O Board design by Alba

PandABox II Firmware



https://www.techway.com/p/optical-fmc-samtec-firefly/

https://www.caenels.com/product/fmc-pico-1m4/



https://www.d-tacq.com/acq427elf.shtml

- Support for additional features:
  - Moving from Diamond rootfs to Yocto
  - 8x bi-directional encoder channels
  - Fine delay (10 ps resolution) on selected digital outputs
  - 1 MHz table based position generator for synthesizing encoder signals
  - 1 MHz table based position compare for triggering detectors based on encoder position
  - 16 MGT channels
    - 4 attached to the SFPs carrier board
    - 12 to FMC for use with Techway Tiger FMC
  - Custom control loops incorporating AI/ML trained models
  - EtherCAT master on PS (still under discussion)
  - Additional FMC :
    - Caenels : FMC-PICO-1M4
    - ACQ427 (with optimized latency block)

Summary and next steps

SOLEIL II
La science éclaire l'avenir
Science lights up the future

Collaborations

Task leadership	DIAMOND	SOLEIL	MAXIV	DESY	ALBA
Schematic Design		√			√
PCB Layout		√			√
Mechanics				√	
FPGA Zynq Processor Design	√		√		
FPGA Zynq Logic Design	√		√		√
Linux Kernel Development	√			(√)	
Linux Application Development	√				
TANGO interface		√	√		
EPICS interface	√				

- Collaboration well established
  - A strong collaboration has been established, fostering shared experience and joint development between facilities.
- Open Source & Open Hardware
  - The platform remains fully open source and open hardware:
    - PandaBox II GitLab Wiki
    - PandaBlocks on GitHub
- Versatile Platform
  - PandABox II is a flexible platform, well-suited for A multipurpose platform for multi-technique scanning and feedback applications[1] across our facilities.
- Ecosystem Integration
  - PandABox II is fully integrated into several control system ecosystems:
  - **Control Frameworks:** TANGO, EPICS
  - **Experiment Control:** SARDANA, BLUESKY, SOLEIL Flyscan

S. Zhang *et al.*,paper TUAPL05, https://doi.org/10.18429/JACoW-ICALEPCS2017-TUAPL05, 2018.

Next step

- Full hardware prototype validated by early 2026
- Firmware and software integration by mid-2026
- Collaboration meetings with users in 2026 at SOLEIL

Happy to meet new users in a collaborative and friendly atmosphere !

- Vendors adoption
  - Quantum detectors in UK
    - https://quantumdetectors.com/products/beamline-data-acquisition-tool/
  - EMG2 in France (Coming soon, discussion ongoing)
    - https://emg2.com/

Acknowledgements

Y-M. Abiven
A.Ammar
J.Bisou
G. B. Christian
T.Cobb
A. Cousins
J.Avila Abellan
X. Serra-Gallifa
V. Main
L. Pithan
O.Seeck
I.Schwark
P. Sjöblom

Acknowledgment to I. Uzun, S. Zhang, G.Renaud, G. Thibaux, F. Langlois, C.Turner, C.Colborne and M. Abott for their contributions to the initial development of PandABox.

SOLEIL II
La science éclaire l'avenir
Science lights up the future

Questions


merci
thank you
gracias
obrigado
danke
go raibh maith agat
спасибо
grazie
sukriya
bedankt
arigatô
ngiyabonga
terima kasih
dziękuję
謝謝
ありがとう
мерси
barka
tau
dakujem
mochchakkeram
teşekkür ederim
hvala
sagolun
chokrane
tapadh
takk
mauruuru
kia ora
grazzi
dėkuji
tanemirt
mersi
diolch
dhanyavad
shukriya
spas
welalin
enkosi
gratias ago
misaotra
matondo
dhanyavadagalu
krap
leat
nandri
mahalo
didi madloba
kop khun krap
mercé
rahmet
taiku
nanni
kam sah hamnida
faafetai lava
paldies
najis tuke
kop khun
mamnun
trugarez
asante
vinaka
Баярлалаа
ευχαριστώ
xiexie
dankie
kiitos
sobodi
dankon
manana
murakoze
tenki
mèsi
blagodaram
хвала
köszönöm
tack
sulpay
akun
aciū
bayarlalaa
djiere dieuf
rahmat
chnorakaloutioun
dank je
gràcies
grâcie
teşekkü ederim