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PandABox II: A COLLABORATIVE PLATFORM DESIGNED FOR FUTURE UPGRADES

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Abstract

Ten years ago, the PandABox platform was first introduced in Melbourne during the MOCRAF workshop. Originally developed through a collaboration between Synchrotron SOLEIL and Diamond Light Source, PandABox was designed to support multi-technique scanning and feedback applications.

Since then, the platform has been widely adopted across synchrotron facilities worldwide—including SOLEIL, DIAMOND, MAX IV, and DESY in Europe; NSLS-II in the United States; HEPS in Asia; and SESAME in Middle East.

With the fourth-generation light sources, there is an increasing need for high-performance, multi-channel encoder processing to enable synchronized data acquisition and motion control during continuous scanning experiments—now a critical feature for automation.

In response to these evolving demands and following discussions within the LEAPS-INNOV WP5.3 project, the opportunity to jointly develop a new state-of-the-art equipment became evident. This effort has since expanded into a broader collaboration that now includes MAX IV, ALBA, and DESY alongside the original partners

This paper presents the new generation of the PandABox platform, offering a comprehensive overview of its integration within EPICS and TANGO control systems. It also outlines future functionalities and the framework of the ongoing international collaboration driving its development.

PANDABOX COLLABORATION

After 10 years of reliable service, an upgrade of the PandABox became necessary. At the same time, discussions began among facilities within the scope of LEAPS INNOV to develop advanced synchronization features for fourth-generation light sources. In this context, experts in synchronization between mechatronics and acquisition systems decided to join forces in developing an upgraded version of the PandABox. The objective is to enhance the platform with greater processing capabilities and new features to support future applications in synchrotron facilities.

PandABox II represents the next step in the evolution of the original PandABox project. This platform builds on the expertise and experience of five synchrotrons—SOLEIL, DIAMOND, MAX IV, ALBA, and DESY—to deliver a more robust, standardized, and versatile solution. It is designed as a multi-purpose platform for multi-technique scanning and feedback applications.

Given its wide adoption and role as a collaborative framework, an agreement has been established to set up active collaboration with core members for governance of the development. Contributing members will share and co-develop new hardware, firmware, and software features for the upgraded PandABox.

EXISTING APPLICATIONS-BASED PandABox

Since the implementation of PandABox, several appli cations have been developed, while others were identified during its evolution. Among these main applications, four are depicted below.

FlyScan Synchronization

The main purpose of PandABox is to generate synchronization signals for data acquisition during continuous experimental scans [1] (Fig. 1).

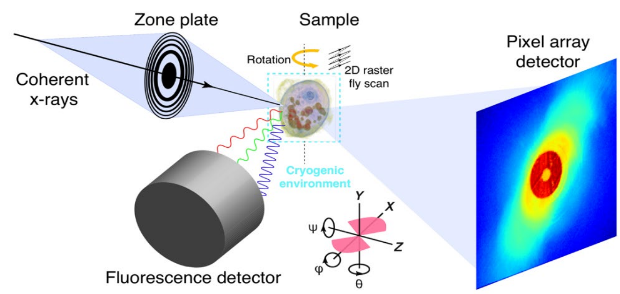

Figure 1: Experimental schematics for simultaneous x-ray flurescence and diffraction measurement [2].

As part of the triggering acquisition platform for Fly-scanning, PandABox is also used for application such as :

- Capture of the QEXAFS monochromator position and ionization chamber signals
- Strain gauge measurements for the fatigue testing machine
- Position capture of nanoprobe interferometers

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Accelerators Current Injection Efficiency and Lifetime Measurement

At SOLEIL, an acquisition system has been developed for the storage ring beam current monitor illustrated in Fig. 2. It is based on the co-developed PandBox electronics, combined with a 24-bit ADC operating at 125 kS/s. The system supports fast, triggered acquisitions (3 Hz), allowing measurement of the injected current even during burst-mode injections.

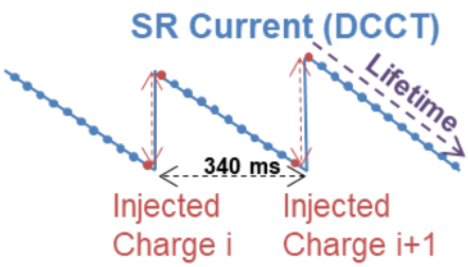

Figure 2: Fast current injection measurement.

Real-time Control System for the Fast Beam-Attenuation with an XPAD x-Ray Detector

To overcome the maximum count-rate limitation, a major constraint of state-of-the-art hybrid pixel detectors, a fast beam-attenuation system was developed at SOLEIL. This fully autonomous system enables dynamic adjustment of the beam attenuation based on the photon flux detected by the XPAD S140 detector.

The system is composed of three main elements in addition to the detector: the XPAD 2D intensity analyzer, the control board, and two sets of attenuating foils, as illustrated in the Fig. 3.

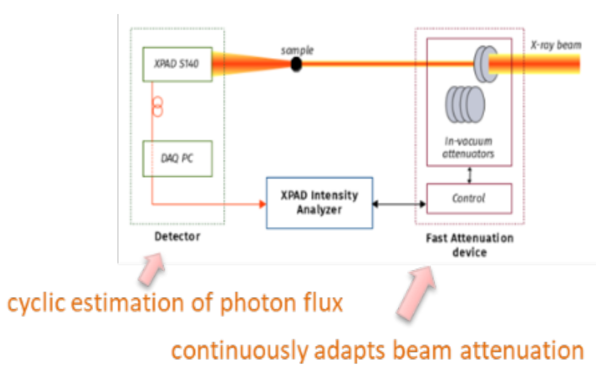

Figure 3: Fast Attenuation system.

Pixel Detector Based on PandABlock Firmware

The overall objective of the project was to design and implement a complete data acquisition system for a detector prototype based on the UFXC32k readout chip for Pump and Probe-probe Experiment as depicted in Fig. 4.

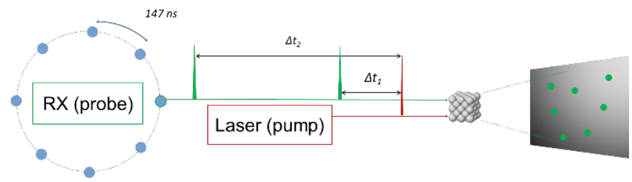

Figure 4: Pomp probe experiment.

To achieve this, the main development focused on the creation of dedicated FMC and SFP FPGA blocks within the PandABlocks [3] framework, specifically tailored to operate on the DAQ box [4].

The hardware architecture (Fig. 5) consisted of three key components:

- The detector prototype, designed to host a two-chip hybrid pixel module.
- The DAQ (Data Acquisition) box, serving as the readout electronics, implemented as a compact hardware variation of the PandABox.
- A server, responsible for slow-control operations and for storing the high-throughput experimental data.

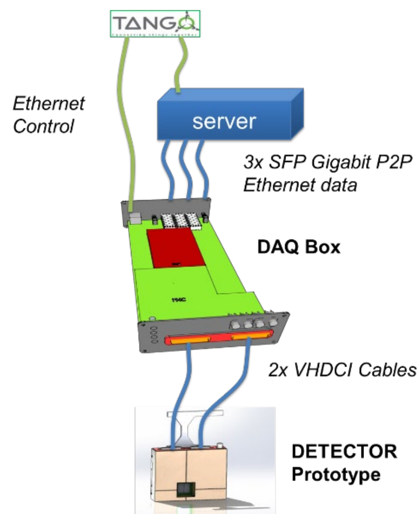

Figure 5: Hardware architecture.

PANDABOX II DESIGN ORGANIZATION

The development of PandABox II is guided by several key principles. The platform is designed to be accessible and straightforward to operate for all collaboration members.

Work is distributed among partners (Table 1) with the objective of creating a complete, turnkey solution that allows rapid and seamless installation of all hardware and software components.

To ensure efficient collaboration and knowledge exchange, structured bi-weekly meetings were organized. During these meetings, each partner systematically reported on the progress achieved, outlined upcoming tasks, and presented the technical challenges encountered, which were then jointly analyzed and resolved within the consortium. as well as sharing minutes and documentation over a private Gitlab repository.

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Table 1: Task Sharing Between Project Partners

Task leadership	DIAMOND	SOLEIL	MAXIV	DESY	ALBA
Schematic Design		√			√
PCB Layout		√			√
Mechanics				√	
FPGA Zynq Processor Design	√		√		
FPGA Zynq Logic Design	√		√		√
Linux Kernel Development	√			(√)	
Linux Application Development	√				
TANGO interface		√	√		
EPICS interface	√				

The PandABox II has not yet been validated for production, as the project is still in the integration and testing phase. Once validated, the project will remain in open source for software and hardware.be shared under the CERN Open Hardware (OHW) [5].

HARDWARE ARCHITECTURE

The PandA II platform is designed around an Enclustra module, and based on this choice, the following architecture, depicted in Fig. 6; is adopted for the design.

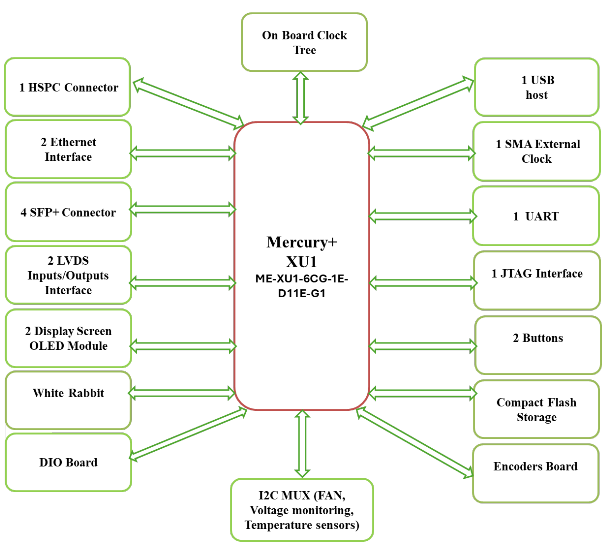

Figure 6: PandABox II hardware global architecture.

- The PandA II platform integrates two LVDS drivers and receivers, providing fast and reliable communication with external devices that require high-speed differential signaling. 4 SFP+ Gigabit transceiver channels, with the fourth port specifically dedicated to the White Rabbit protocol [6], ensuring highly precise and stable time distribution for synchronization.
- The High-Speed Serial Pin Connector (HSPC) [7] enables interfacing with both commercial analog and digital boards, as well as custom I/O modules. It also supports the integration of the TigerFMC Firefly [8] module or any FMC module with 12 MGT on the PandA II platform.The system is equipped with two Gigabit Ethernet links: the first dedicated to integration with control systems, and the second reserved for new features such as System management interface or as an EtherCAT master depending on the facility or the applications
- The DIO Board (equipped with LEMO and BNC connectors) and the Encoder Board (providing eight input/output channels and supporting several standards such as Incremental, Absolute, EnDat, and BiSS), (Fig. 7). On the main board, a 50-pin connector provides the interface to connect these boards with the Mercury module.

Figure 7: On top the DIO board prototype and below the Encoder board prototype.

- 2 Display screen OLED module are used to show slow-changing diagnostic information, updated at 1Hz by the PS. One for the front panel and one for the rear panel.

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- The interfaces with I²C bus include: 4SFP+, FMC+, DIO Board, Encoders Board, 2 clock generators, voltage monitoring, temperature sensors, 2 display screens.

At the heart of the system architecture is the Enclustra Mercury+ XU1(ME-XU1-6CG-1E-D11E-G1) system-on-chip (SoC) [9], as shown in Fig. 8. This module is designed to provide a comprehensive set of features essential for diverse embedded processing applications, including memory, configuration interfaces, Ethernet, USB, and clock management. It offers convenient access to over 294 user I/O pins through 200 FPGA I/Os. For this project, the “G1” assembly variant is utilized. The “G1” variant provides 16 GTH MGT lines on the module connector, with the trade-off of reducing the number of standard FPGA I/Os to 180 instead of 200.

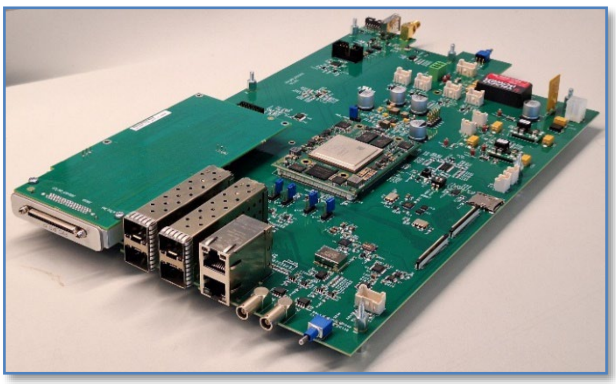

Figure 8:First prototype of the carrier board with Enclustra Mercury+ XU1 Top.

The clocking circuitry is designed for maximum flexibility. The system clock can be sourced from the PS subsystem, an MGT-recovered clock, or an external clock provided through an SMA connector. The PandA II can operate as a White Rabbit endpoint using any of the front-panel SFPs. The MGT reference clocks may be supplied by either of the two on-board programmable oscillators, oscillators on an FMC+ card, or a high precision DAC-controlled oscillator when operating in White Rabbit mode.

PandA II will consist of a 1U or 3U metal enclosure, equipped with two switchable boards (DIO board and encoder board) and two Gigabit Ethernet ports on the front panel.

PANDABOX II

I/O and Mechanical Integration

This new version is designed with a 241.3 mm carrier board supporting the processor. This size allow the design of 2 form factors rack, the board can fit in a 19’’, 1U rack as shown on Fig. 9 as well as an 3U but half 19’’ rack.

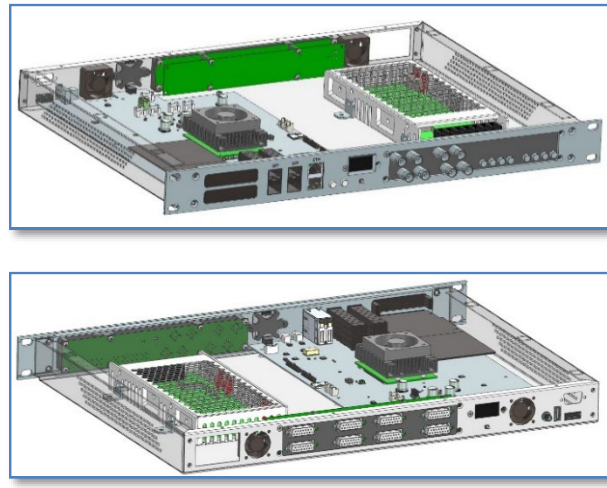

Figure 9: 3D CAD of the PandABox II showing the front and back panel.

The features on the existing PandABox will be maintain.The rear panel connectors are identically maintain, with 8x 15-way D-type connectors which can be configured as input or output. The USB, JTAG and serial console terminal for linux acces over RS232 serial port.

The Front Panel is sligthly changed including:

- 4x SFP (Small Form-factor Pluggable) sockets providing modular interfaces that can easily adapt to various fiber optics and copper networking standards by connecting compact and hot-pluggable SFP transceiver module to one socket.
- 16 Multi-Channel TTL and LVDS I/Os for synchronous triggering and clocking signals via BNC and LEMO connectors.
- 2x Gigabit Ethernet connector for control system integration, high-speed data acquisition and future implementation of Ethercat feature.
- 1 display for status, IP configuration

The onboard FMC slot is updated from LPC (Low-Pin Count) connector to LPC with the 12 MGT of the enclustra board mapped on the connector.

FIRMWARE CAPABILITIES

The firmware for the original PandABox is provided by the PandABlocks project [10]. This consists of the FPGA firmware and an embedded Linux rootfs running a TCP server for control and data acquisition and a webserver for interactive setup. The updated PandABox II will be supported by the same project, keeping a common set of functionality between the two platforms. The project provides a set of run-time rewirable functional blocks for digital pulse and position creation, compare and capture at rates up to 1MHz. This rate was judged sufficient at present, with the additional SFP ports allowing a faster data transfer in the future if necessary.

PandABox II contains a 4x larger FPGA, which will allow the firmware to support the additional features the hardware supports:

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- 8x bi-directional encoder channels
- Fine delay (10 ps resolution) on selected digital outputs
- 1 MHz table based position generator for synthesizing encoder signals
- 1 MHz table based position compare for triggering detectors based on encoder position
- 16 MGT channels which only 4 are used for the actual SFPs and 12 to the FMC.
- Custom control loops incorporating AI/ML trained models

To better support both platforms and ease future maintenance by the expanded collaboration, the custom rootfs is being ported to Yocto. This enables more flexible system where packages can be pulled in from upstream to a single larger rootfs that is able to load different firmware based on the currently connected FMC card.

SOFTWARE INTEGRATION

Software integration is done via a connection to the TCP server running on the PandABox and this is unchanged for PandABox II. To ease integration a pandablocks python library [11] allows commandline and scripting interface to a PandABox.

To provide an EPICS interface, the pandablocks python library is wrapped using the FastCS framework [12]. This project introspects the available functional blocks that a particular PandABox supports, and creates PVs for all of them. It also provides an introspection structure to levels above like bluesky [13] so that they can do the same. As well as allowing getting, setting and monitoring the value of all fields, the EPICS interface also supports writing HDF files from the data captured by the PandABox.

To provide a Tango interface, depicted in the architecture Fig. 10, FastCS can also be used as it has provisional Tango support. Initially, however, the existing Tango device server from SOLEIL will be used.

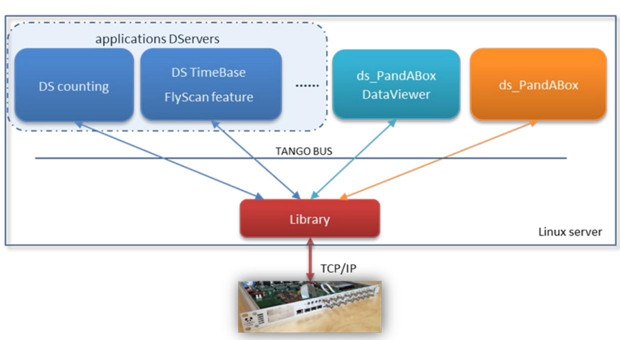

Figure 10: Tango communication architecture.

Three types of TANGO Device Servers (DServers) are currently used:

- Hardware PandABox DServer – for configuring and monitoring the PandABox hardware.
- Generic PandABoxDataViewer DServer – designed to support customizable user interfaces.
- Application-specific DServers – tailored for dedicated use cases.

The PandABoxDataViewer DServer will undergo some changes to split its functionality into two separate components: one for configuration and the other for data acquisition.

MAX IV, is using the community PandABlocks library and developped a custom PandABlock layout for each beamline; the layout has to be custom due to different needs and equipment to be integrated. Even for common techniques such as XAS (spectroscopy) where continuous mono-id scans are used, there is the need to integrate different equipment. As an example, the Hippie beamline[14] needs an additional chopper integrated at the scan frequency, whereas the Flexpes beamline needs support for manipulator scans.

Tango is used as a control system and Sardana as a scan orchestrator. Since the PandABox layouts are different, a dedicated way of interfacing PandABox is needed. As a result, MAX IV also has a dedicated Tango device and/or Sardana controller to interact with PandABox in a different procedure.

Basically, we can classify PandABox into two different instruments: master clock and data acquisition. As a master clock for timing, MAX IV generally uses MRF EVR events (100 MHz bunch RF frequency), but PandABox has the ability to trigger on sub-harmonics of it, and in other cases PandABox acts as the master clock itself. As data acquisition for encoder counts for energy, position reconstruction based on the scan frequency, or detector as a pulse counter replacing e.g. NI6602 at finest and ADlink cards for general analog voltage reading.

This dual use made MAX IV create two different device controllers: one for timing and one for data acquisition.

The layout is version controlled by the control system code, and check-up is done searching for modifications before every scan. The user is warned if any difference is detected; this guarantees the integrity of the system.

CONCLUSION

All individual components of the PandABox II have been purchased to build the first prototype and validate the new design. Full validation is expected by the end of 2025.

As mentioned before, new firmware feature are already identified such as Low Current monitor in order to control DCM pitch modulation and feedback to improve long term X-ray beam stability or power supply control for fast corrector on the SOLEIL II.The collaboration agreement includes an annual workshop with all developers and users of the platform. The goal is to share experiences with both the platform itself and the results from its various applications. Another objective is to discuss and gather requests for new developments in terms of hardware, firmware, and software. The first PandABox collaboration meeting will be held next year at SOLEIL.

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