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THE ESS FAST BEAM INTERLOCK SYSTEM - DESIGN, DEPLOYMENT AND COMMISSIONING OF THE NORMAL CONDUCTING LINAC

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Abstract

The European Spallation Source (ESS) is a research facility based in Lund, Sweden. Its linac will have an high peak current of 62.5 mA and long pulse length of 2.86 ms with a repetition rate of 14 Hz. The Fast Beam Interlock System (FBIS), as core system of the Beam Interlock System at ESS, is a critical system for ensuring the safe and reliable operation of the ESS machine. It is a modular and distributed system. FBIS will collect data from all relevant accelerator and target systems through 300 direct inputs and decides whether beam operation can start or must stop. The FBIS operates at high data speed and requires low-latency decision-making capability to avoid introducing delays and to ensure the protection of the accelerator. This is achieved through two main hardware blocks equipped with FPGA based boards: a mTCA 'Decision Logic Node' (DLN), executing the protection logic and realizing interfaces to Higher-Level Safety, Timing and EPICS Control Systems. The second block, a cPCI form-factor 'Signal Conversion Unit' (SCU), implements the interface between FBIS inputs/outputs and DLNs. In this paper we present the implementation of the FBIS control system, the integration of different hardware and software components and a summary on its performance during the latest beam commissioning phase to DTL4 Faraday Cup in 2023. s

INTRODUCTION

ESS [1], located in Lund, Sweden, is on the forefront of neutron science research. ESS has designed its Machine Protection system [2,3] to strike a delicate balance between safeguarding equipment from potential damage and ensuring high beam availability. This equilibrium is of paramount importance due to the unprecedented proton beam power of 125 MW per pulse (with an average of 5 MW). Uncontrolled release of this energy could result in catastrophic damage to equipment within microseconds. To address this critical concern, ESS has developed the FBIS, which is engineered for minimal latency. The FBIS plays a pivotal role in ESS operations, tasked with collecting a diverse range of data from various Sensor Systems, including both slow systems such as Vacuum, Magnets, Personal Safety System (PSS) as well as fast systems like Radio Frequency Control Local Protection System and Beam Instrumentation. These data inputs serve as vital signals for processing units (PU) within the FBIS, which are responsible for making real-time decisions on whether to continue or halt beam production, thereby ensuring the safe and reliable operation of the ESS accelerator.

ARCHITECTURE OF FBIS

The FBIS architecture is fully redundant to ensure it can reach the Protection Integrity Level requested by the Protection Functions. It was developed by a team constituted of the ESS in-kind partner ZHAW [4], the ESS electronic standard manufacturer IOxOS Technologies [5], and ESS FBIS team. Hundreads of Sensor Systems connection are foreseen along the 600 m Linac, leading to a specific architecture with two component types: the "Signal Conversion Unit" (SCU) and the "Decision Logic Node" (DLN).

Signal Conversion Unit (SCU)

The SCU, Fig. 1, is a concentrator for Sensor Systems connections. It is based on a cPCI standard chassis with custom electronic cards. An SCU hosts up to 12 Mezzanine Cards (MC) on which Sensor Systems connect. Two more cards, called Serializers, host a MPSoC Zynq Ultrascale+ to manage the connection to the MC by the backplane, and the communication with the DLN through serial links (Slink), redundant optical connections using the Xilinx Aurora 64b/66b core IP.

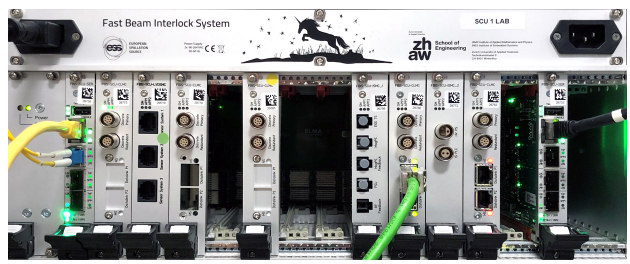

Figure 1: Signal Conversion Unit - SCU.

Several kind of MC were designed to interface with various types of Sensor Systems. One of them manages PLC-based Sensor Systems [6], and two others fast electronic Sensor Systems, mainly FPGA-based. Twenty five SCUs are foreseen along the Linac and in the Target building. The two first SCUs, installed close to the Ion Source, host also specific MC to interface with five hardware Actuators, acting to stop the Beam Production upon DLNs request.

Decision Logic Node (DLN)

The DLN, as depicted in Fig. 2, is responsible for implementing the protection logic utilized by the FBIS. Furthermore, it facilitates connections to the Higher-Level Safety System, Control System, and the ESS Timing System. The

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DLN is built upon the mTCA standard and employs a 3U chassis to accommodate the redundant IFC1410 Intelligent FMC Carrier AMC [5], which serves as the core component for FBIS functionality. It receives data from the SCUs via the Rear Transition Module (RTM) using the Slink communication protocol, while also exchanging status information with other DLNs through the Optical Protection Line (OPL). In addition to this, the crates house the Timing System Event Receiver (EVR) [7] and a Concurrent CPU, which hosts EPICS Control System IOCs.

Figure 2: Decision Logic Node - DLN.

The protection logic, implemented in FPGA, is written in VHDL. Each DLN receives data from the SLink and direct it along parametrized routes set during synthesis to different Processing Units (PUs).

Given different types of input signals the purpose of the signal processing units is to compute a unified representation known as a Decision Logic Variable (DLV). Every PU's DLV can trigger actions like Beam Inhibit (BI), Regular Beam Interlock (RBI), or Emergency Beam Interlock (EBI). These Beam Switch-off requests are propagated along the OPL, optical connections between all DLNs and both SCUs hosting actuator MCs which use this information for decision on interrupting beam production.

So far the different types of PUs are:

- SPU (Signal PU): This unit computes DLVs representing OK, NOK, and ERROR states of input signals. Depending on its parametrization, on the Proton Beam Mode (PBM) and on Proton Beam Destination (PBD), the SPU can be latched to detect and store signal states, masked by the operator and filter out in order to be excluded from further data processing.
- PBSPU (Proton Beam signal PU): This unit compares PBM and PBD signals with requested values. The comparison results in a DLV, with masking used to force the comparison result to be OK and filtering to exclude safe situations from DLF processing.
- SSPU (State Supervision PU): This unit checks the reaction of Actuator Systems to FBIS Beam Switch-Off Requests. If checks fail, it can escalate to an EBI. The Global Beam Permit is used as a reference for this processing.
- SWSPU (Software PU): This unit translates register values into DLVs, allowing operators or applications to trigger Software BI, Software RBI, or Software EBI actions.

The DLVs, as well as the signal states and their parametrizations can be read out via registers. These registers are a means of accessing the DLV values and signal states for further use or monitoring.

CONTROL SYSTEM

The Integrated Control System for ESS is based on the EPICS framework. As described above both DLNs and SCUs are FPGA based systems. They have different register access and different registers mapping. DLN is based on proprietary network on chip : TOSCA by IOxOS instead of SCU is based on AXI peripheral register access. To simplify management, we integrated FPGAs using StreamDevice support and a software daemon. This intermediary layer enhances FPGA integration into the EPICS control system, enabling seamless data exchange between the FPGA and the control system. This flexibility is crucial as FPGAs in DLN and SCUs use different protocols. Software daemons and IOCs via streamdevice facilitate periodic FPGA register reading for monitoring input systems, system status, and health monitoring.

This approach ensures efficient communication, real-time responsiveness, customization, centralized control and comprehensive monitoring.

In addition DLNs and SCUs contain a rolling History Buffer (HB) of the latest 1023 events that occurred. Each event is represent by a 128-bits record with heterogeneous information (precise timestamp, type of event, etc). An example of these information are shown in Fig. 3. In the firmware, it is represented as a RAM object using 16kB. The control system can also read these HB on request, the one of SCUs being focus on interface signals, the one of DLNs mostly to understand the sequence of events during particular situation, especially after unclear Beam Stops or during commissioning.

Date	ns	SuperType	GBP	EBI	RBI	BI	Type	SubType	Signal
2023-06-26 13:54:26	710,000,623.6	BSO					GBP	OK	
2023-06-26 13:57:59	843,698,577.4	PU DLV out					SPU	4	NOK
2023-06-26 13:57:59	843,698,577.4	PU DLV out					SPU	5	NOK
2023-06-26 13:57:59	843,698,585.6	BSO					Local BI	NOK	
2023-06-26 13:57:59	843,698,593.8	BSO					Local RBI	NOK	
2023-06-26 13:57:59	843,698,602.0	BSO					GBP	NOK	
2023-06-26 14:02:06	716,866,002.9	PU DLV out					SPU	4	OK
2023-06-26 14:02:06	716,867,387.4	PU DLV out					SPU	5	OK
2023-06-26 14:02:06	716,867,395.6	BSO					Local BI	OK	
2023-06-26 14:02:06	716,867,395.6	BSO					Local RBI	OK	
2023-06-26 14:02:06	716,870,475.8	BSO					GBP	OK	

Figure 3: History Buffer.

SCU

An SCU can host up to 12 MCs, therefore each Serializer registers mapping structure is divided into different main blocks: one for the global configuration, one for each MC slot and one for the Slink. These details are summarized in an overview OPI, Fig. 4. With all slots filled, an SCU Serializer has a set of 800 registers. The MC registers are organized into generic categories: read only for monitoring purpose, read/write for control, and write only to reset, rearm or clear counters. These generic registers contain different kind of information depending on the MC type. The EPICS control system needs to know which type of MC is installed on which slot to decode them properly.

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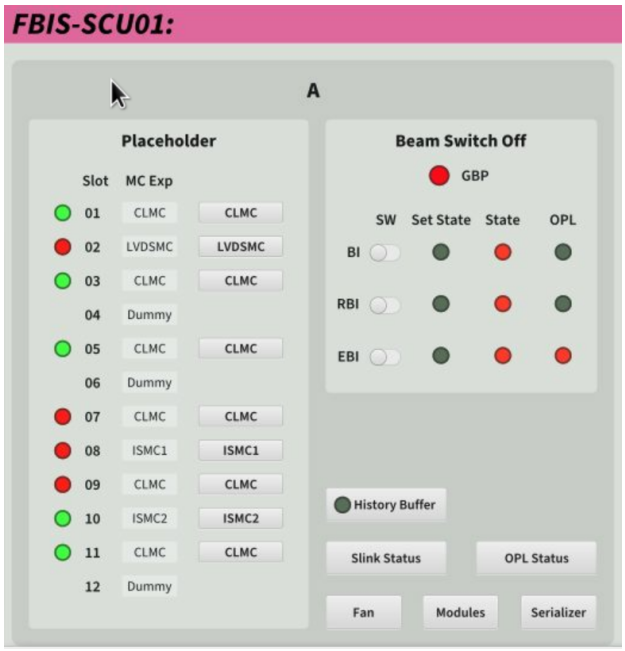

Figure 4: SCU main OPI.

The Serializer processor part hosts the Xilinx proprietary embedded Linux called Petalinux. This allowed developing a powerful c++ based software daemon by ZHAW, able to manage the monitoring and control of the FBIS SCU critical parameters (status or overriding of signals like Beam Permits, etc), and realizing the crate management through interface with I2C devices and GPIOs.

This software makes asynchronous the clients requests (from EPICS control system or other) and the firmware or crate management readings and writings. It communicates with the clients through TCP protocol, well handled by Streamdevice on the EPICS control side.

DLN

The number of registers to be read depends on the parametrization of the DLN, specifically for the number of Slinks and the number of PUs. In the worst-case scenario, there are approximately one thousand registers that need to be read. However, periodically reading this many individual registers poses challenges for StreamDevice.

To address this issue, we have organized the registers into two distinct groups within the Input/Output Controllers (IOCs), each represented by a waveform. The first group comprises registers that need to be read only once, primarily containing information related to the system's parametrization. For instance, these registers may indicate whether an SPU is maskable, the applicable proton beam modes, and the destination for proton beams. Operators can look at this through the OPI shown in Fig. 5.

The second group includes registers that require periodic reading. These registers encompass various functionalities, such as monitoring the status of Slinks, Optical Protection Lines (OPL), or reading the values of inputs both before and after masking or filtering processes have been applied.

In addition to managing registers, the DLN IOC also plays a crucial role in reading Process Variables (PVs) from the Event Receiver (EVR) of the timing system. Subsequently, it writes these values into the FPGA registers. This process involves updating operational parameters determined by the operator, including proton beam mode, proton beam destination, and beam status (beam on/off).

Figure 5: DLN OPI. SPUs details.

FBIS

EPICS IOCs for DLNs are hardware-oriented, typically comprehensible only to system owners and experts. To address the need for a more operator-friendly approach, we introduced the concept of input systems. For FBIS, examples of input systems include Protection Safety System (PSS), MPS PLC Systems, RF systems ... In example FBIS incorporates two inputs related to PSS, namely "Beam Permit" and "Redundant Beam Permit." What we require is a mechanism to consolidate these two signals. Operators should be able to determine if PSS is in an acceptable state by checking the status of both inputs. Additionally, they should have the capability to mask PSS with a single action, such as pressing a dedicated button. As shown in Fig. 6.

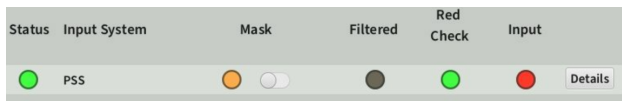

Figure 6: FBIS OPI with details about PSS.

Furthermore, since FBIS operates redundantly, operators must ensure that PSS is functioning correctly by verifying the status of both inputs, which are read by two serializers in the SCU and processed by two different IFC1410 boards in the DLN.

During each commissioning phase, FBIS undergoes configuration changes, often involving the addition of more sensor systems. This means that the values of high-level PVs, frequently accessed by operators, may require recalculations involving additional factors or changes to the PVs used in the computation.

This high level EPICS IOC is capable of both retrieving and configuring PVs across all DLNs EPICS IOCs. The PVs are shown to operators using the OPI of Fig. 7.

COMMISSIONING AND OPERATION

Deployment

The FBIS for the full Linac is constituted of 7 mTCA DLNs and 25 cPCI SCUs as in Fig. 8. For the Normal

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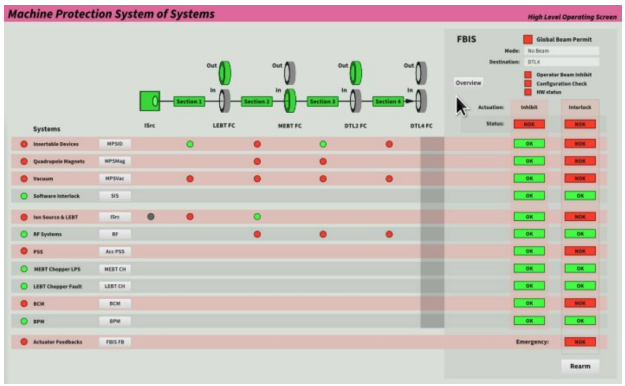

Figure 7: FBIS top level OPI.

Conducting Linac (NCL) commissioning phase to DTL4 Faraday Cup (FC), a subset of 2 DLNs and 4 SCUs was installed.

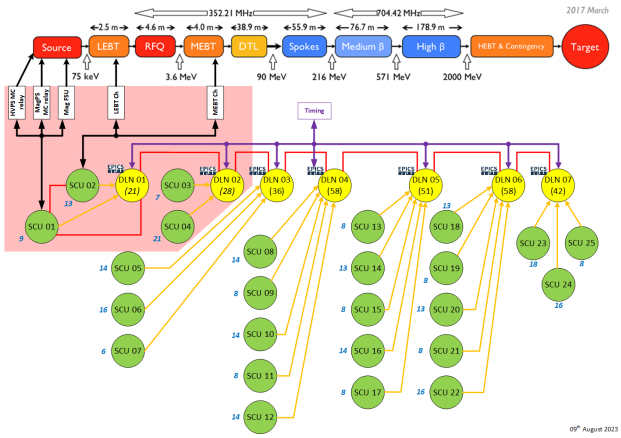

Figure 8: FBIS full deployment with DTL4 FC installation highlighted.

SIT

The Site Integration Test (SIT) is conducted after all lab Factory Acceptance Tests (FAT) for hardware and firmware validation (FAT Unit and FAT integration), and after the system has been installed on site. It consists of 2 main parts:

- I/O tests (see Fig. 9) to check that all signals provided by each sensor system are connected to the right place, and considered as the proper signals by the DLN logic. Each signal is affected a type of PU (SPU, PBDSPU, etc) with an index in the DLN logic. When a signal state is changed, the test checks the correct PU is affected.

Table 02: BCM

#	Section 01 - Interface: Interfacing device signal name (DDS document)	Section 02 - FBIS SCU: SCU	MC type	SCU slot	MC port	Cable Nb	Section 03 - FBIS DLN: DLN	PU	BSO type	Result chan A (term + OPI)	Result chan B (term + OPI)	Ref No.
	BCM1					168034537						
	(Discrete Signals)					N/A						
1	Beam Absent	FBIS-SCU01	LVDSMC	2	1	N/A	FBIS-DLN01	SPU 2, 3 SSPU 0	N/A	Pass / Fail	Pass / Fail	☐ N/A
2	Beam Permit	FBIS-SCU01	LVDSMC	2	1	N/A	FBIS-DLN01	SPU 4	RBI	Pass / Fail	Pass / Fail	☐ N/A
3	Ready	FBIS-SCU01	LVDSMC	2	1	N/A	FBIS-DLN01	SPU 5	N/A	Pass / Fail	Pass / Fail	☐ N/A
	(Datalink)					N/A						
4	Beam Absent	FBIS-SCU01	LVDSMC	2	1	N/A	FBIS-DLN01	SPU 6, 7	N/A	Pass / Fail	Pass / Fail	☐ N/A

Figure 9: SIT I/O test for BCMs

- Functionality tests (Fig. 10) to check FBIS protection functions logic is working as expected. Mostly to ensure the Global Beam Permit (GBP) is removed in critical circumstances.

	7.1.8. Scenario 7: Software Interlock System					
7.1	Set the FBIS in operational state with GBP OK	FBIS is up and running, GBP OK	As Expected: Yes No	Pass Fail		☐ N/A
7.2	From **MPS SIS OPI** set the SIS **Beam Permit A** to NOK and verify the SIS Beam Permit at locations below. 1. **"MPSoS OPI"** = "Software Interlock" Interlock 2. **"FBIS DLN01: Beam Switch Off A"** - SIS for RBI 3. **"FBIS DLN01: Beam Switch Off B"** - SIS for RBI	1. FBIS is in Regular Beam Interlock state 2. **"MPSoS OPI"** = "Software Interlock" Interlock is Red 3. **"FBIS DLN01: Beam Switch Off A"** - SIS for RBI is Red 4. **"FBIS DLN01: Beam Switch Off B"** - SIS for RBI is Red	As Expected: Yes No	Pass Fail		☐ N/A
7.3	Set back the SIS Beam Permit A to OK and rearm the FBIS	FBIS is up and running, GBP OK	As Expected: Yes No	Pass Fail		☐ N/A

Figure 10: SIT functionality test for the Software Interlock System (SIS).

IOCs

In this commissioning phase we had eigth IOCs for SCUs, four IOCs for DLNs and one FBIS IOC. The deployment and monitoring of IOCs have been carried out using CE, an in-house developed tool at ESS. CE Deploy and Monitor is a Java application with a REST interface. It facilitates the creation, administration, and monitoring of IOCs in a standardized and centralized manner across the ESS network. This is achieved through the utilization of Ansible playbooks. It offers functionality for IOC monitoring and the execution of specific remote procedures.

Statistics

A postmortem (and post-run) analysis was carried out to count, reconstruct, and assign the system's trips and faults of the machine. Although the names of the FBIS inputs do not represent individual systems, they show the conceptual split between the functionalities and a further breakdown was performed. For the purpose of this paper, we focus only on two top-level splits.

During the 91 days of scheduled beam commissioning in 2023 [8] FBIS (along with other systems) was verified and operational at all times. Figure 11 illustrates the percentage of available beam time w.r.t the time when the beam was off due to the FBIS (and/or) operator request. The intended stops were counted for planned accesses and scheduled stops. The time with Beam ON represents time spent with studies on various destinations in the ESS linac.

A further look at the Beam OFF cases can reveal the detailed split by FBIS inputs. Figure 12 depicts the split of all of 4300 various trips. One can see that there is a fair amount (close to 30%) of intended stops, which is not surprising in the days of beam commissioning. The rest (3200 times) is driven by the inconsistent state of the inputs. A big contribution of the trips to FBIS came from the RF input. This is related to the complexity of the vertical systems behind that input. ESS RF systems are interfaced with FBIS via Local Protection Systems (LPS) and those require many subsystems to be in an operational state. Losing any of it causes FBIS input to interlock the GBP. As a result of this analysis, we indicated possible future improvements in terms of recognition of RF input and changing some from

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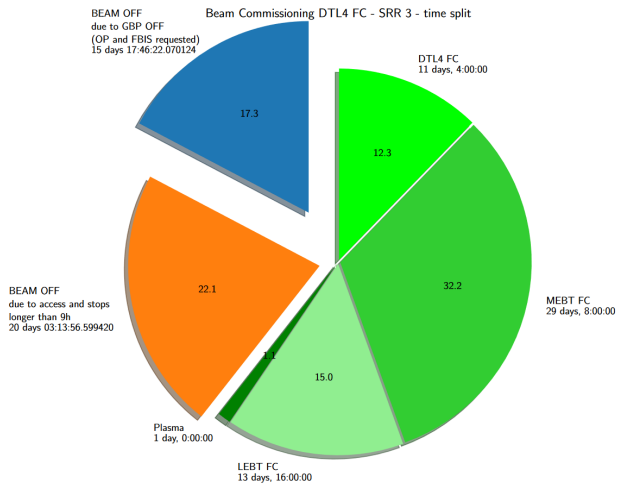

Figure 11: ESS NCL commissioning time split with 17% time off due to the FBIS triggered beam stops.

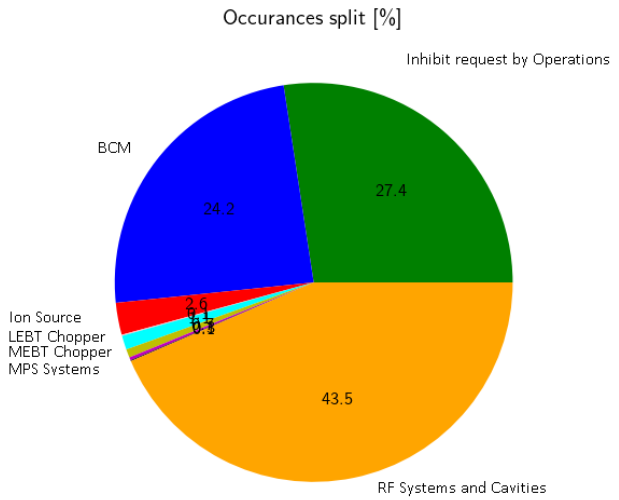

Figure 12: ESS NCL commissioning trips split by the FBIS input. The dominant part is intended by operations usually used for machine configuration adjustments. The next three players are inputs related to the RF systems, Beam Current Monitor, and Ion Source. The remaining ≤ 6% covers all other active inputs.

interlocking to inhibiting. Another important contributor to the FBIS-triggered beam stops is BCM input which governs the produced beam to fulfill the desired (or requested) beam pulse characteristics. Many trips via this channel are the result of the commissioning and validation of protection functionalities and were part of the commissioning plan. Last but not least, the third significant input trigger was found to be Ion source system-related. The remaining trips (260 in total) represent ≤ 6% of all trips and were mainly related to the commissioning character of the studied period. Finally, there were very few cases when the system went into trip mode due to internal faults including three MPS-related inputs. However, these were isolated cases once again reflecting the commissioning sense of the highlighted period.

CONCLUSION

The FBIS has been fully operational for the NCL commissioning to the DTL4 Faraday Cup. Beam stops were triggered when necessary for machine protection purpose, but also in many more circumstances. A rough minimum availability of the machine can be estimated around 60%, considering the ratio between the Beam Off (22.1 % + 17.3% of total time) and the total time of the commissioning. When running in full operation, the machine availability is foreseen to be above 95%. This will be achievable by reducing drastically access time, by reducing the time to restart beam thanks to more advanced post-mortem analysis tools, and by making more use of the inhibit feature of the FBIS that allows automatic recovery of the GBP, in particular for the RF systems.

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