COMMISSIONING OF THE 352MHz TRANSVERSE FEEDBACK SYSTEM AT THE ADVANCED PHOTON SOURCE*

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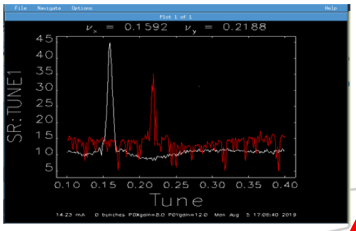
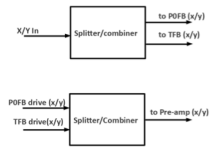
Abstract:

With the success and reliability of the transverse feedback system installed at the Advanced Photon Source (APS), an upgraded version to this system was commissioned in 2019. The previous system operated at a third of the storage-ring bunch capacity, or 432 of the available 1296 bunches. This upgrade samples all 1296 bunches which allowed corrections to be made on any selected bunch in a single storage-ring turn. To facilitate this upgrade the development of a new analog I/O board capable of 352 MHz operation was necessary. This paper discusses some of the challenges associated in processing one bunch out of 1296 bunches and how flexible the system can be in processing all 1296 bunches. We will also report on the performance of this system.

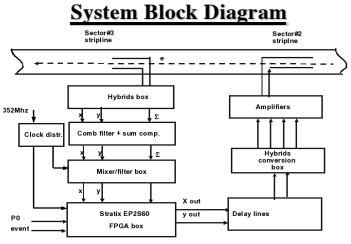


Tune plot of hybrids fill pattern when the loops are optimized



A block diagram of the integration of the new TFB system

System Block Diagram



BlockDiagram of bunch-to-bunch feedback

The front-end input circuit was upgraded from the monopulse receiver to a 3-tap comb filter.

Single Mode Fiber connection, delay of 144ns.

Transverse Feedback – Main Box

Sec 35

Transverse Feedback
– Remote DAC Box
– Current location
– About 188m

Sec 02

Remote Fiber Optic link

Currently the remote DAC is connected via a 2.34 Gb/s fiber optic. The transmitter at the main box is in 16-bit mode while the receiver at the remote DAC box is in 8-bit mode. The 8-bit mode is used to solve two issues, 1) byte swapping that may occur at power-up or if fiber was disconnected and 2) the need to half step the delay value being sent to the remote DAC.

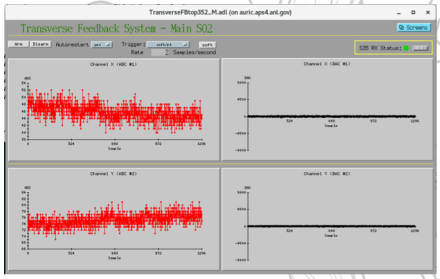
-- Transmitter using 117.333 MHz reference clock.
-- Receiver using 234.666 MHz reference clock.

The Upgrade will transmit 32-bits at 7.04 Gbps

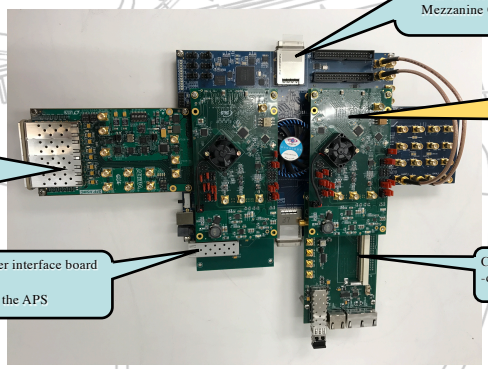
Beam direction

Sec 30

Transverse Feedback
– Remote DAC Box
– Future location
– About 322m



Main control screen for the TFB system.



Terasic TR4 Development Kit Stratix IV GX with six HSMC (High Speed Mezzanine Card) connectors.

SFP Cage adapter board to Four SFP cages transceivers. Four SFP cages LVDS

Will be transmitting at 7.04 Gbps

This 400MSPS Data conversion board is capable of 400 MHz for the analog inputs and 400 MHz for the analog outputs. This board was developed at System Level Solutions (SLS).

Note: two are installed.

Event Receiver interface board HSMC -developed at the APS

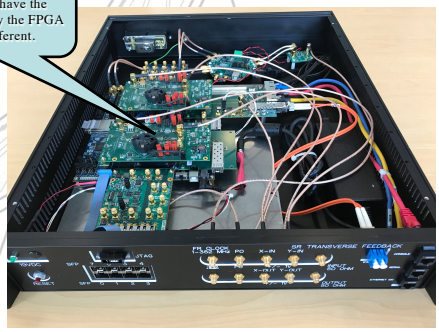
Coldfire daughter board HSMC -developed at the APS

Possible Bucket Modes

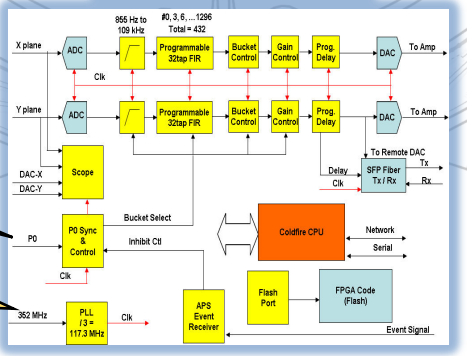
FPGA CLK	Number of buckets that can be sampled
88 MHz	Samples only 324 buckets 1) 324 mode 2) Hybrid mode 3) 648 FIR filters needed
117.3 MHz	Samples only 432 buckets 1) 24 singlet mode 2) Hybrid mode 3) 864 FIR filters needed
352 MHz	Samples all 1296 buckets 1) Any bucket configuration 2) 2392 FIR filters needed

The current configuration is 117.3 MHz.

Completed chassis Both the master and the slave chassis have the same hardware, only the FPGA firmware is different.



FPGA Main Block Diagram



New P0 trigger input circuit needed to clean the jitter and to be synchronized to the 352 MHz source.

New input clock circuit needed to clean the jitter in the 352 MHz source.

1. Storage Ring @ 352MHz, (2.84ns)
2. Bunches/buckets = 1296
3. ADC sampling rate 352 MHz (2.84ns)
   a. Samples all of the buckets.
   b. 1296 buckets can be enabled.
4. Storage Ring turn rate = 271.6kHz (3.68μs)
5. Inputs use 14-bit A/D 400MSPS
6. Output uses 14-bit D/A 400MSPS

Conclusion

We successfully completed the development and testing of transverse feedback system that upgraded the sample rate to 352 MHz, allowing the system to run in all three user operational fill patterns (24 singlet, 1+8x7 hybrids and 324 singlets) and other patterns for machine studies. Both control screens and high-level applications are completed now for user operations.

Transverse Feedback and Remote DAC Hardware

1) Terasic TR4 Development Kit Stratix IV GX
   a) Six HSMC (high speed mezzanine card) connectors
2) SLS 400MSPS Data Conversion HSMC (2 cards installed)
   a) One Analog to Digital converters, 14-bits
   b) One Digital to Analog converters, 14-bits
3) Coldfire CPU daughter board with HSMC connectors.
   a) Fiber optic transceiver used for the event timing system.
   b) Console, serial and Ethernet ports, RJ45
   c) Connector for an RF clock, connected to the FPGA.
   d) User defined SMB connector, 2 inputs and 2 outputs.
4) Transceiver by Finisar, model FTLF1428P2BTL
   a) A 8Gb RoHS Compliant Long-Wavelength SFP Transceiver

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