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LOCAL OSCILLATOR REAR TRANSITION MODULE FOR 704.42 MHz LLRF CONTROL SYSTEM AT ESS*

I. Rutkowski, K. Czuba, M. Grzegrzółka, Warsaw University of Technology, Poland

Abstract

This paper describes the specifications, architecture, and measurements' results of the MTCA-complaint Local Oscillator (LO) Rear Transition Module (RTM) board providing low phase noise clock and heterodyne signals for the 704.42 MHz Low Level Radio Frequency (LLRF) control system at the European Spallation Source (ESS). The clock generation and LO synthesis circuits are based on the module presented at ICALEPCS 2017. The conditioning circuits for the input and output signals must simultaneously achieve the desired impedance matching, spectral purity, output power as well as the phase noise requirements. The reference conditioning circuit presents an additional challenge due to input power range being significantly wider than the output range. The circuits monitoring the power levels of critical signals and voltages of supply rails for remote diagnostics as well as the programmable logic devices used to set the operating parameters via Zone3 connector are described.

INTRODUCTION

Modern linear particle accelerators subject charged subatomic particles (or ions) to electormagnetic field in order to increase their energy. A Low Level Radio Frequency (LLRF) control system stabilizes the electromagnetic field inside accelerating modules using the amplitudes and phases of the cavity RF signals detected by down-converting them to an intermediate frequency. The signals are then sampled and digitized by high-speed precise analog-to-digital converters. The architecture necessitates synthesis of clock and LO signals. Quality of those signals influences the performance of the field detection.

The European Spallation Source (ESS) LLRF control system is based on the Micro-Telecommunications Computing Architecture (MTCA) [1]. The two aforementioned signals are generated by the LO board having a rear transition module (RTM) form factor and supplying 4 neighboring LLRF systems [2]. Important parts of the design are based on a module designed for the Cavity Simulator project [3] known as CS-LOG and described in [4].

The next section lists requirements of the LO-RTM project.

REQUIREMENTS

The input reference frequency is 704.42 MHz and the nominal input power is +3 dBm ± 2 dB. The clock to reference frequency ratio is 1/6 and the IF to reference frequency ratio is 1/28 or 1/22 (corresponing to 117.40 MHz and 25.16 or 32.02 MHz, respectively). LO and clock signals' phase noise requirements are presented in Table 1 and they are dependent on the sufficient quality of the reference signal. Other requirements:

- compliant with the MTCA.4 RTM specification,
- form factor: RTM (mid-size or full-size),
- combined power good signal for all power supply voltages and information about board temperature shall be provided to the MTCA.4 management,
- 1 reference output (power level: +13 dBm ± 1 dB),
- 4 main LO outputs (power level: +15 dBm ± 1 dB),
- 4 main clock outputs (power level: +15 dBm ± 1 dB),
- the main signals connector type: SMA,
- 1 monitoring LO output and 1 monitoring clock output (power level: > -20 dBm),
- the monitoring output signals connectors type: MMCX,
- RF signals connectors' location: front panel,
- clock and LO signals spectrum: sine waves with maximum harmonic spurious level of -60 dBc,
- the non-harmonic spurious not greater than -60 dBc for clock and not greater than -50 dB for LO,
- the VSWR on each port (Reference Input, LO Outputs, CLK Outputs) not greater than 1.5 (corresponding to return loss of -14.0 dB),
- the maximum absolute error of the power detection: 1 dB,
- resolution of power detection: 0.05 dB or better,
- the module shall be controlled by the AMC module through Zone3 connector,
- the pinout of the Zone3 connector: compliant with the DESY digital class D.1.0 [5],
- 1 clock signal shall be provided at the Zone3 connector,
- Zone3 signaling standard: LVDS,

DESIGN

This section describes circuits introduced in LO-RTM to fulfill the new requirements.

LO Signal Conditioning and Distribution

The selection of LO frequency synthesis scheme as well as selection of the IF divider and amplifier were presented in [4]. Direct Analog synthesis scheme was selected for the design because it introduces no systemic frequency error and reduces the far-from-carrier uncorrelated phase noise.

The circuit verified on CS-LOG was modified to achieve the desired output power level at 4 outputs. A 1W HBT linear amplifier is used as the final driving stage in addition to the low-noise preamplifier (see Fig. 1). An attenuator sets the second stage's point of operation. A coupler and resistive power divider provide signal to the power detector and the monitoring output.

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Table 1: Phase Noise Performance Requirements

Offset (Hz)**:**	10	100	1k	10k	100 k	1M	10 M
LO Phase noise SPD $\left(\frac{\text{dBc}}{\sqrt{(\text{Hz})}}\right)$**:**	-90	-110	-125	-140	-149	-152	-154
Clock Phase noise SPD $\left(\frac{\text{dBc}}{\sqrt{(\text{Hz})}}\right)$**:**	-104	-120	-130	-140	-145	-150	-153

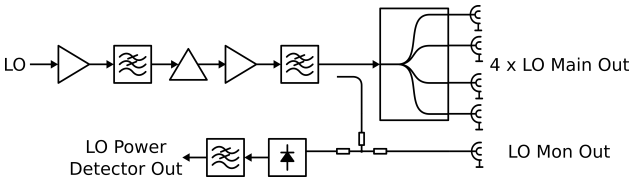

Figure 1: A simplified schematic of the LO signal conditioning and distribution circuit.

Clock Signal Conditioning and Distribution

The clock signal power conditioning circuit was changed to provide the higher output power at 4 outputs. The operation amplifier was replaced with a wideband HEMT unit. Similarly to the LO circuit a coupler and a resistive power divider were added (see Fig. 2).

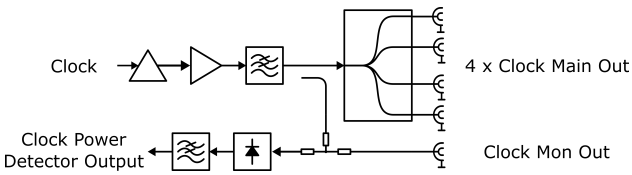

Figure 2: A simplified schematic of the clock signal conditioning and distribution circuit.

Reference Signal Conditioning and Distribution

The reference input power dynamic range of -2 dB to +2 dB must be compressed to -1 dB to +1 dB at the output. This can be done either by controling gain of the signal distribution circuit by external loop or by using non-linear characteristics of devices making up the circuit. The second approach was taken since it is safer (doesn't depend on proper operation of the stabilizing loop) and requieres less component.

Two actions were taken in order to minimize leakage of the mixing products to the main reference output. The isolation between output ports of the two-way power divider was maximized and two parallel amplifiers were used instead of one after this divider (see Fig. 3).

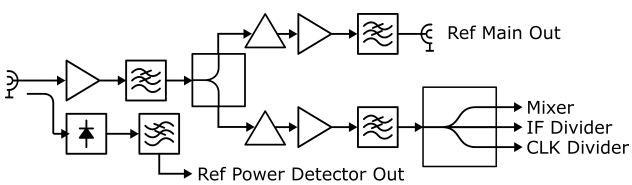

Figure 3: A simplified schematic of the reference signal conditioning and distribution circuit.

Power Levels' Monitoring

All three distribution signals are equipped with a logarithmic power detector. The detector' output voltages are low-pass filtered and amplified to match the whole input range of the ADC digitzing the signals. A very small refresh rate is assumed, making sampling frequency unimportant. The converter was selected to fulfil the resolution and absolute error requirements.

Digital Logic

On the CS-LOG a microcontroller was used to configure all the on-board integrated circuits. The requirements concerning the Zone3 communication and LVDS signaling render the microcontroller unsuitable as currently available microcontrollers support LVDS standard only for communication with a display. A Programmable Logic Device (PLD) from the MachXO2 [6] family manufactured by Lattice Semiconductor was selected based on:

- number of IO pins needed,
- supported signaling standards,
- number of required different power supply voltage rails,
- presence of build-in configuration memory,
- presence of build-in oscillator,
- price.

Due to low amount of data transfered between the RTM and a AMC module the Serial Peripheral Interface (SPI) was selected as the communication protocol. Two out of eight 8-bit registers are writeable, while the other six contain read-only values of detected power levels.

TESTS AND MEASUREMENTS

Three revisions of LO-RTM were designed, produced, assembled, and tested. A mirrored land pattern of the main DC/DC power converted rendered revision 1.0 unsuable. It was tested with additional external power supply bypassing the converter. The power level of the clock's second and third harmonics was too high. Revision 1.1 was operational, a stronger low-pass filter improved the the clock's spectrum, but some of the requirements were still not meet:

- the return loss at the LO outputs was too small,
- the output power of the LO signal was outside the specified range for extreme reference signal's input power values.

Lumped components were placed at each port of the LO signal's power divider to improve the impedance matching. A fixed attenuator between LO signal's amplifiers (see Fig. 1) was replaced with a programmable one, allowing to adjust the output power to the desired value.

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15 pieces of revision 1.2 were manufactured and assembled. Before connecting to the power supply they were visually inspected. No defects were detected during the inspection. All boards passed the test and the results of measurements were similar, therefore results for only oneboard (see Fig. 4) are presented. The reference input is visible in the bottom-left corner. The LO (in the middle) and the clock (top) sections are seperated to minimize interference.

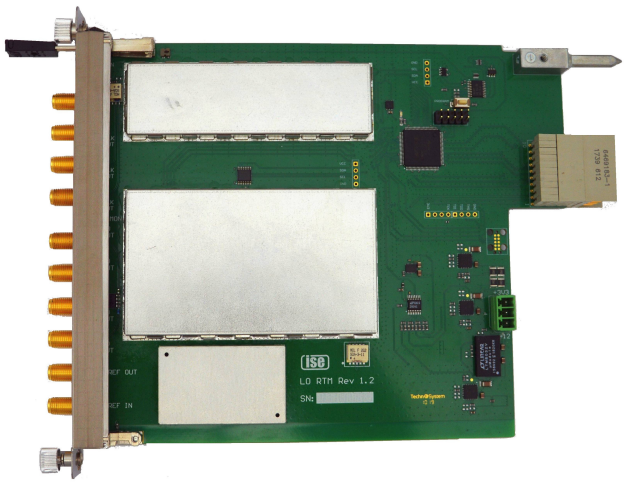

Figure 4: Picture of an assembled LO-RTM board.

Spectrum

The output power of the LO signal varies with the input power and can be controlled by changing the intermediate attenautor settings. The LO signal spectrum was measured as a function of the input power and attenuation for two IFs and two IF signal standards. Figure 5 shows power of the LO signal fundamental (dBm) and Fig. 6 ilustrates the power of 5th harmonic (the strongest according to measurements) relative to the fundamental. For operating conditions complying with the output power requirement the SFDR criteria is also satisfied.

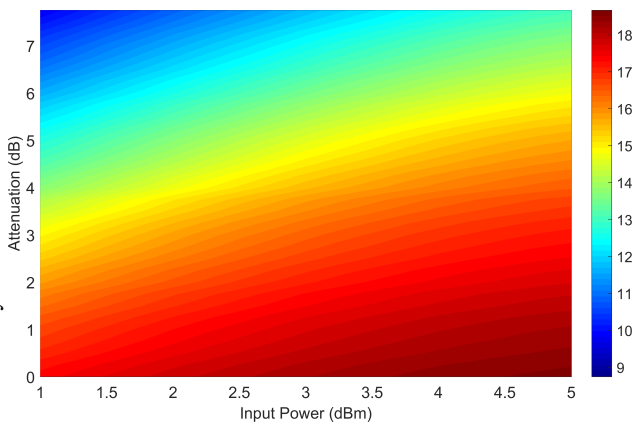

Figure 5: Power of LO signal's fundamental (dBm) as a function of the input power and attenuation.

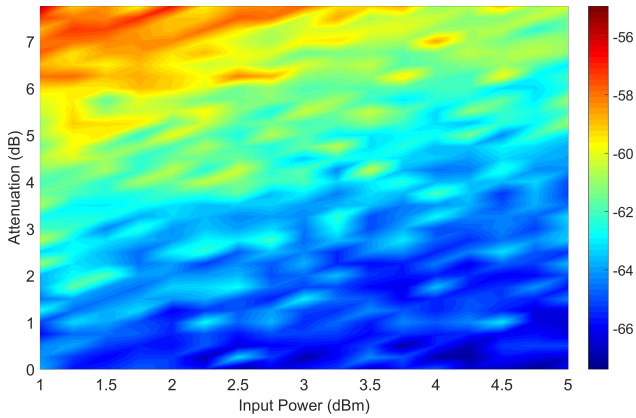

Figure 6: Power of LO signal's 5th harmonic (dBc) as a function of the input power and attenuation.

The spectrum of the clock signal (see Fig. 7) is independent of the input power, can not be chnaged by software, and meets all the requirements.

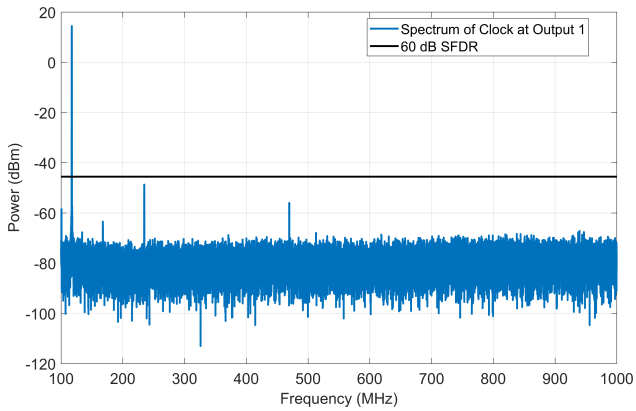

Figure 7: Clock signals spectrum at clock output 1.

Impedance Matching

Impedance matching at a given port was measured with all other ports terminated. The clock ports' matching meets the requirements (see Table 2).

Table 2: Clock Ports' Reflectivity at 117.4 MHz

Channel	Value [db]
1	-16.87
2	-17.73
3	-18.14
4	-17.94

The reflectivity at the LO port varies strongly as the function of frequency due to filter's characteristic in the passband (see Fig. 8). The LO ports' reflection coefficients fulfill the specification.

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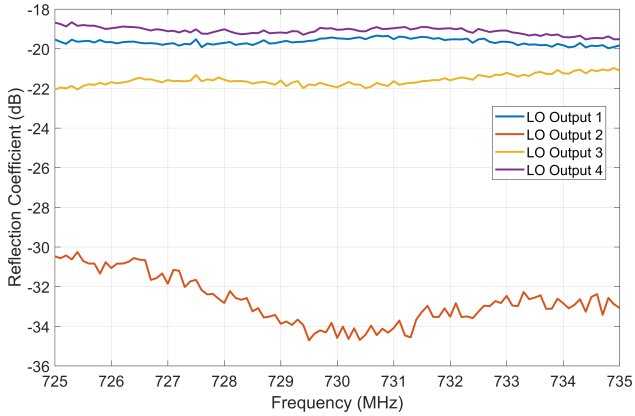

Figure 8: Magnitude of reflection coefficient measured at the LO ports.

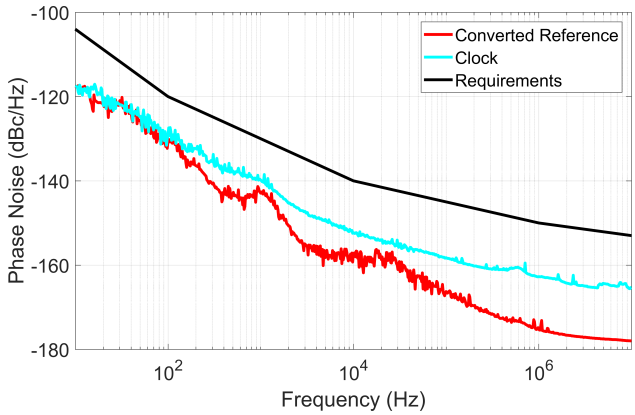

Figure 9: Phase noise spectra of the clock signal, an ideally converted reference signal, and requirements. Division ratio: 6, input frequency: 117.40 MHz MHz.

Phase Noise

The phase noise of both the clock and the LO signals (see Figs. 9 and 10) is significantly lower than the specified maximum.

CONCLUSION

The requirements, architecture, and measurements results of the LO generation board were presented. The LO-RTM revision 1.2 meets all requirements. The first batch is expected to be installed at ESS in 2020. Based on experience gained

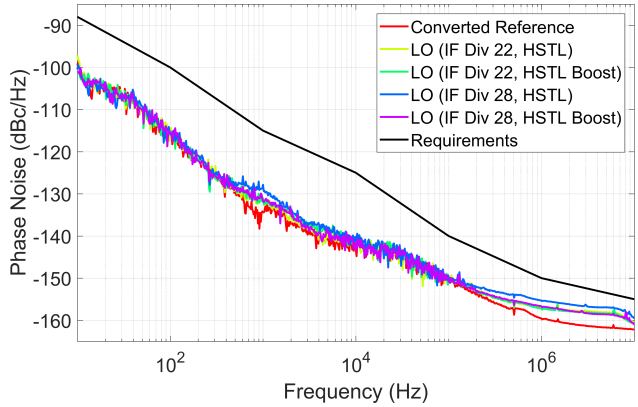

Figure 10: Phase noise spectra of an ideally converted reference signal and the LO signal (two IFs and two signaling standards).

a new revision with minor improvments might be dsigned or more boards of the revision 1.2 will be manufactured.

REFERENCES

[1] A. J. Johansson, A. Svensson, F. Kristensen, and R. Zeng, "LLRF System for the ESS Proton Accelerator", in *Proc. 5th Int. Particle Accelerator Conf. (IPAC'14)*, Dresden, Germany, Jun. 2014, pp. 2465–2467. doi:10.18429/JACoW-IPAC2014-WEPME079

[2] J. Szewinski *et al.*, "Contribution to the ESS LLRF System by Polish Electronic Group" in *Proc. 8th Int. Particle Accelerator Conf. (IPAC'17)*, Copenhagen, Denmark, May 2017, pp. 4026–4027. doi:10.18429/JACoW-IPAC2017-THPAB129

[3] M. Grzegrzółłka, K. Czuba, and I. Rutkowski, "Cavity simulator for European Spallation Source", *IEEE Transactions on Nuclear Science*, vol. 66, no. 7, pp. 1254-1261, July 2019. doi:10.1109/TNS.2019.2890994

[4] I. Rutkowski, K. Czuba, M. Grzegrzółka, "LO board for 704.42 MHz cavity simulator for ESS", in *Proc. 16th Int. Conf. on Accelerator and Large Experimental Physics Control Systems (ICALEPCS'17)*, Barcelona, Spain, Oct. 2017, pp. 1573–1576. doi:10.18429/JACoW-ICALEPCS2017-THPHA081

[5] https://techlab.desy.de/support/zone_3_recommendation/index_eng.html

[6] https://www.latticesemi.com/Products/FPGAandCPLD/MachXO2.aspx