

MACHINE PROTECTION SYSTEM FOR HIAF

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Abstract

The High Intensity Heavy-ion Accelerator Facility (HIAF), currently under construction, is a complex machine that couples a Continuous Wave (CW) superconducting ion Linear accelerator (iLinac) with a high-energy synchrotron to produce various stable and radioactive intense beams with high energies. The machine has a versatile operation mode which requires a high flexibility and reliability to the Machine Protection System (MPS). A customized and robust MPS is designed and developed to give the readiness of the machine for operation, to mitigate and analyze faults related to the relative damage potential. To get a high speed and have a high level of reliability, all interlock signal processing is processed on radiation-tolerant Field-Programmable Gate Arrays (FPGA) with triple or dual redundancy, as well as with a fail-safe design. By implementing a multiprocessing platform system-on-chip FPGA, the HIAF MPS can be tightly integrated with other systems to maximize availability pinpoint failures for operations, and give the post-mortem analysis. This paper will describe the architecture of the interlocks linking the protection systems, the strategies to manage the complexity, the detailed components, and the interlock logic of the customized HIAF MPS, as well as the test and verification of the prototype.

INTRODUCTION

The High Intensity Heavy-ion Accelerator Facility (HIAF) [1, 2] is a next-generation research facility for heavy-ion science and technology, the layout is as the Fig. 1 shown. HIAF consists of SECR (superconducting electron-cyclotron-resonance ion source), iLinac (ion Linear Accelerator), BRing (Booster Ring), HFRS (HIAF fragment separator), SRing (spectrometer ring) and several experimental terminals. The main beam parameters of HIAF are shown in Table 1.

The iLinac has three types of beam operation modes. CW mode is mainly used to supply beam between the iLinac and the T1 terminal, pulse mode is mainly used between the iLinac and the BRing, and the splitting time, in which the two ion sources supply beams and the iLinac accelerates the two types of beams in time to the T1 terminal and the BRing. The operation of the BRing is characterised by the complexity of the operation modes, the complexity of the beam structure, and the fast rate of up-conversion. The speed of BRing is fast. These pose challenges for the design of MPS.

The whole machine is split into 13 sections and the logic of the MPS is to combine different sections to meet

different operation modes. To have a high flexibility, the whole accelerator is partitioned by 2 master controllers master and 8 slave controllers slave. Depending on the mode of operation, different protection strategies are developed to protect the relevant beam supply areas, and interlock signals can be provided to the corresponding ion source and chopper according to the operating conditions.

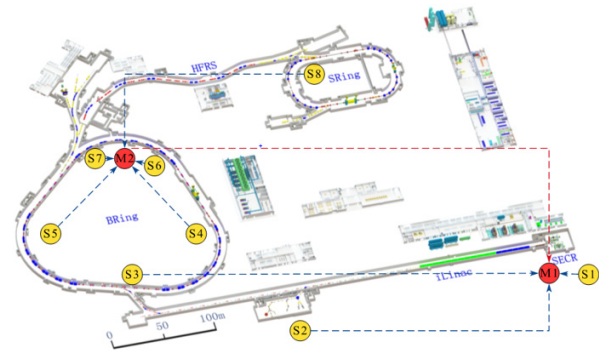


Figure 1: Layout of the HIAF.

Table 1: Overview of MPS of Several Accelerators

	SECR	iLinac	BRing	SRing
Length / circumference (m)		114	569	277
Beam energy of U (MeV/u)	0.014	17	835	800
Beam intensity of U	50 μ A	28 μ A	2×10^{11} ppp	$(0.5-1) \times 10^{12}$ ppp
Operation mode	DC	CW or pulse	fast ramping (12 T/s, 3Hz)	DC, deceleration

High-energy, high intensity beams that pose a significant threat to materials and equipment. Calculations based on the beam parameters of the HIAF indicate that the power of the DC uranium beam at 1 emA, 17 MeV/u is 115.6 kJ. The thermal deposition effect of the uranium beam on the stainless steel at a beam profile of σ of 2 mm will cause the stainless steel to rise to 1398 °C at 28.8 μ s, close to the melting point, as shown in Fig. 2.

To ensure a safe machine operation, especially for the CW superconducting linac, HIAF MPS needs to have a very fast response and the beam mitigation should respond within 20 μ s after receiving NOK inputs. In addition, there are many operation modes at the HIAF complex, the MPS should be able to handle a large number of devices, feature configurable responses, possess signal logging for PM analysis, and must have a high level of reliability and flexibility, and so pose unique design challenges. Because of

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its versatile operation modes and complicated requirements, no commercial off-the-shelf equipment can meet the demands of HIAF MPS, thus a flexible, reliable, distributed, and fast MPS system is designed and investigated.

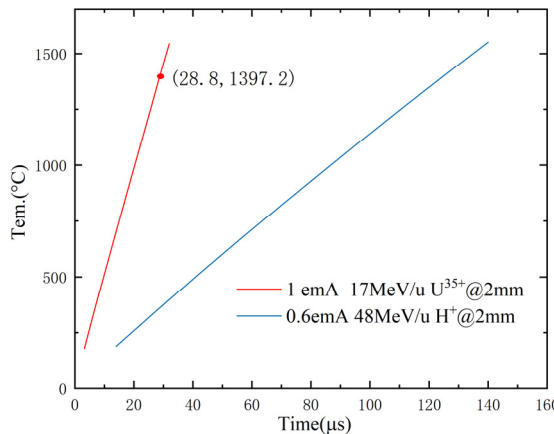


Figure 2: Thermal effects on stainless steel by beam.

HIAF MPS

For the time division and zone operation mode, the tree structure is mainly adopted as the main body of the whole machine protection system as the Fig. 3 shown. According to the operation mode, different protection strategies are formulated to protect the relevant beam supply area, and interlock signals can be provided to the corresponding ion source chopper. According to the characteristics of the BRing, the ring structure is used to connect the interlocking fan-out electronics, as the main implementation scheme of the beam current dump system, the magnet power supply and radio frequency system synchronously give the dump signal.

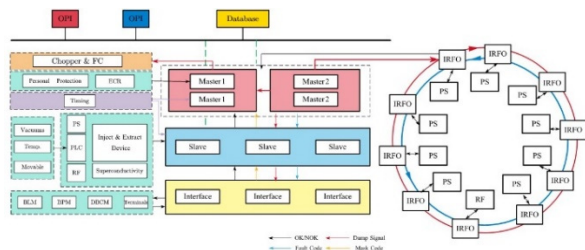


Figure 3: Overview on the HIAF MPS framework.

The masters, the slaves and the interfaces formed a three-layer tree structure. The master and the interlocking fan-outs form a daisy-chained ring structure. interface adopts a triple-redundant design, mainly accessing the interlocking signals from the beam diagnostic equipment BPM, BLM and BCM, and then connecting to the slave after logical determination. Slave also adopts a triple-redundant design, collecting the signal from the interface and the interlocking signals from the power supply, radio frequency, injection extraction system and the PLC (Programmable Logic Controller) controller of the slow protection system. Master is a dual redundant design, collecting signals from the slave and the highest priority systems such as the ion source and the personal protection system.

In the end, all signals from the slave controllers will be collected to the master controller layer to be processed and give a global beam operation permit signal, and beam dump request, as well as to provide the evidence as a first call for event analysis and assist the operator for the post analysis. In addition, the access system goes directly to the master controller which results in a beam abort and inhibit when personnel are inside potentially dangerous parts of the accelerator complex.

Hardware

The MPS hardware consist of three types of electronics: interface electronics, master/slave controller electronics and interlocking fan-out electronics, respectively.

The hardware of the interface electronics is shown in Fig. 4. To achieve high speed and get a high level of reliability and flexibility, all signal processing on the interface is accomplished with triple modular redundancy (TMR) technique, by using three FPGA chips working independently. In case the interface is located inside the tunnel and constantly in a radiation environment, the radiation-hardened A3P1000 [3] from ProASIC3 Flash Family FPGAs is chosen because it is a flash-based device.

- Radiation-resistant FPGA: ProASIC3
- Triple module redundancy.
- Fibre-optic communication (10 MHz/20 MHz).

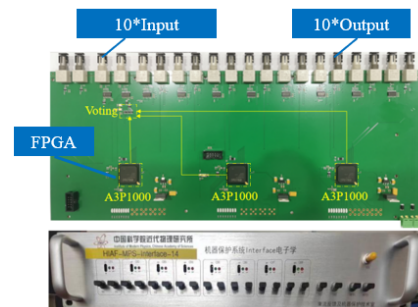


Figure 4: The interface electronics hardware.

The Master/Slave electronics hardware as the Fig. 5 and Fig. 6 shown. The master and slave share a common hardware design. Master/slave controller is designed in a customised 6U chassis, the main part includes power supply, 9 digital front-end boards (DFE) and one main control board (MCB as the Fig. 6 shown). Adopting A3P1000 anti-radiation chip and FPGA XCZU15EG [4] with ARM, each DFE can access 4 channels of user devices and supports optical fibre and Ethernet communication.

- Xilinx XCZU15EG
- ARM cortex-A53
- 16 GB SO-DIMM DDR4
- FMC connector for White Rabbit.

The interlocking fan-out electronics hardware as the Fig. 7 shown. The main function is to fan out the interlocking signal to the power supply and radio frequency system in the Bring. It can feedback the working status of the power supply controller and self-test in the link. Ring interlock fan out are daisy-chained, using a clockwise and

anti-clockwise double-loop circuit, using a modular design of the Manchester encoding method.



Figure 5: The Master/Slave electronics hardware.

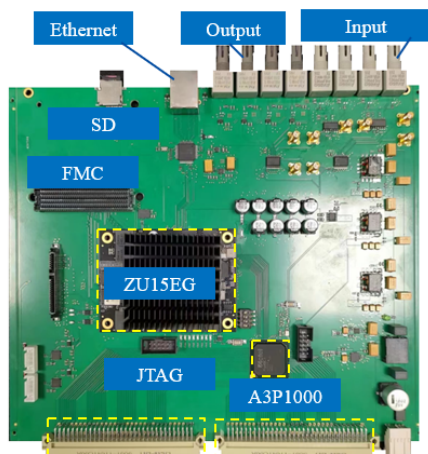


Figure 6: The MCB electronics hardware.



Figure 7: The interlocking fan-out electronics hardware.

Firmware and Software

The master/slave electronics is mainly composed of MCB and DFE. 9 DFEs interact with MCB for interlocking signals and data at the same time through the high-speed plug-in backplane. A3P1000 is used as the logic chip on the DFE board, which is responsible for collecting the interlocking signals and fault information of the sub-devices, and sends them to the MCB board after decoding and encoding at the same time. There are two FPGA chips on the MCB, one is the radiation-resistant A3P1000 to perform the logic interlock function, and the other is the ZU15 with ARM to be responsible for the data interaction with the upper layer. A3P1000 is the core of the local interlocking

logic processing, and acts as an intermediate hub for uploading the status of the equipment and sending the interlocking strategy.

The data communication between MCB and DFE adopts the customised SPI bus method as the Fig. 8 shown. The frame clock CNV and bit clock DCO are provided by the logic chip on the MCB, and the frame transfer rate is 1 MHz, and the bit rate is 100 MHz. 8 data lines and two clock lines are connected between each DFE and the MCB, and each frame contains 64 available bit data. and the interlock signals occupy a separate channel.

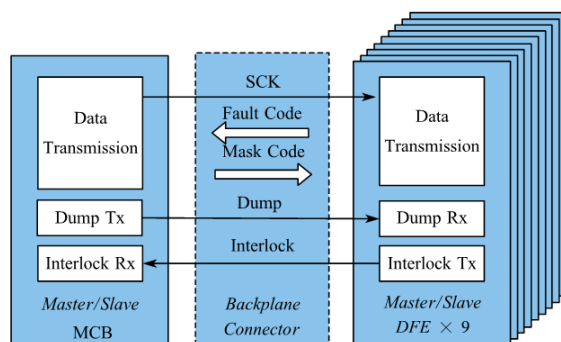


Figure 8: Communication between MCB and DFEs.

The logical block diagram of the programme module is shown in Fig. 9. When used as slave or master, the procedure is slightly different. The red dash line in the Fig. 9 indicates that it is used as a slave.

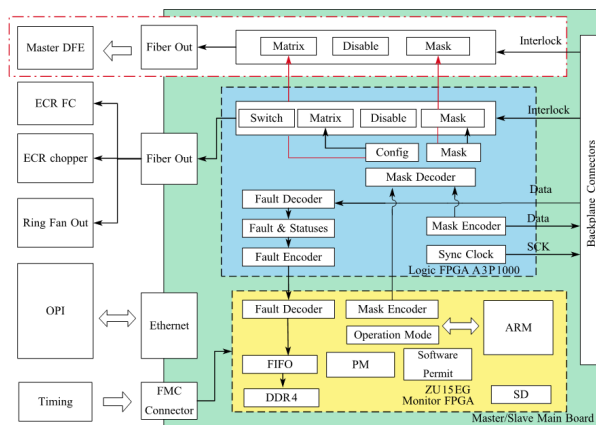


Figure 9: The logic framework of the slave/master main controller board.

The interlocking logic is implemented in the logic FPGA A3P1000 as the blue block in the Fig. 9, which mainly completes the collection and giving of fibre optic signals for various hard connections. In the monitoring FPGA using ZYNQ IP core to complete the design of the system on chip as the yellow block in the Fig. 9, through the AXI4 bus to complete the PL side and PS side of the data transfer, can use the BRAM for interlocking information locking, integrated with the EPICS [5] architecture to complete the release of the PV. Various soft signals, including soft interlock, timestamp, and interlock status data are done on the monitoring FPGA-ZU15.

MPS must provide the possibility to trace back to the origin of an event and transmit the control index to the junior device. A fault code is defined for uploading the status of the primary device as well as the self-test signal, a mask is defined for sending down the control parameters, and the mask states. To ensure the security and stability of the mask transmission in a radiation environment, Manchester encoding is used for data transmission. At the same time, a CRC check digit is added to ensure the reliability of the data.

Prototype

The HIAF MPS prototype is built for performance demonstration as the Fig. 10, which include differential current monitor (DCM) electronics for the interlock input, interface electronics, a slave, and a master controller. The interface collects the user interlock signal from the DCM electronics. The MPS response time is about $4.6 \mu\text{s}$ for the whole system, as displayed in Fig. 11. The yellow wave is the interlock input from the DCM, and the green is a dump signal from the master controller.

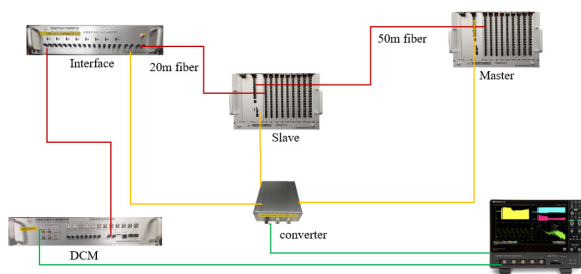


Figure 10: Test platform of prototype.

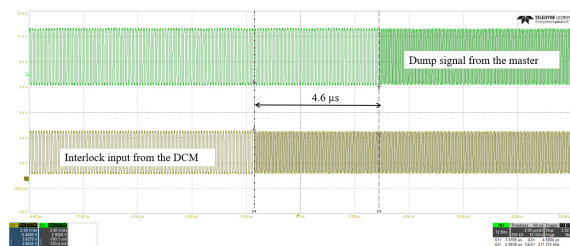


Figure 11: The response measured of the MPS system.

CONCLUSION

The HIAF MPS system prototype is built and the function is verified, which meets the project requirements. As HIAF complex functions in many different operating modes, the complete MPS must be flexible and configurable, and support local and global responses. The interlock logic is distributed, thus the MPS can be seamlessly expandable when systems are added to the protected machine, which is especially useful during system-by-system commission. The MPS can be configured to offer the possibility to mask any input channel to facilitate the operation of the machine, which allows the entire system to implement different behaviour in different machine modes. By implementing the triple redundancy to make the decision and double redundancy to abort the beam, as well as the fail-safe design, failures of the MPS hardware itself can be effectively mitigated. The whole system is highly reliable with high speed in $4.6 \mu\text{s}$ from OK/NOK inputs to mitigation outputs, which meets our requirements. However, system integration into the HIAF complex and commission challenges lay ahead.

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