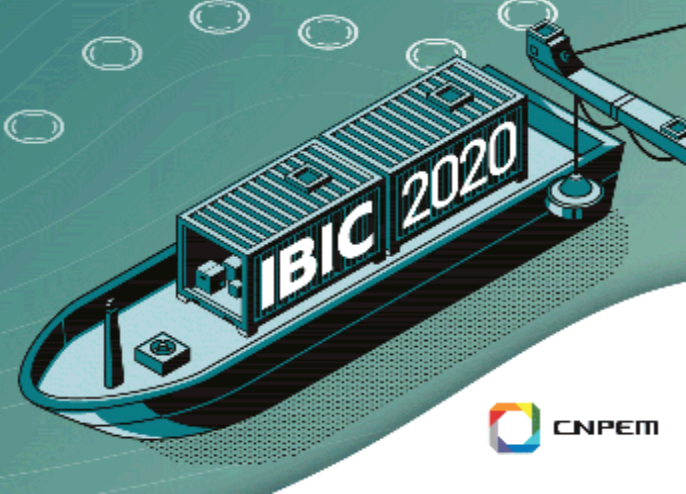


**Brazil**

**14 - 18**

**September**



# Brief Introduction to HEPS BPM Electronics Development

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Beam Instrumentation Group, IHEP, CAS, China

September 14-18 2020

IBIC2020, Brazil

# Outline

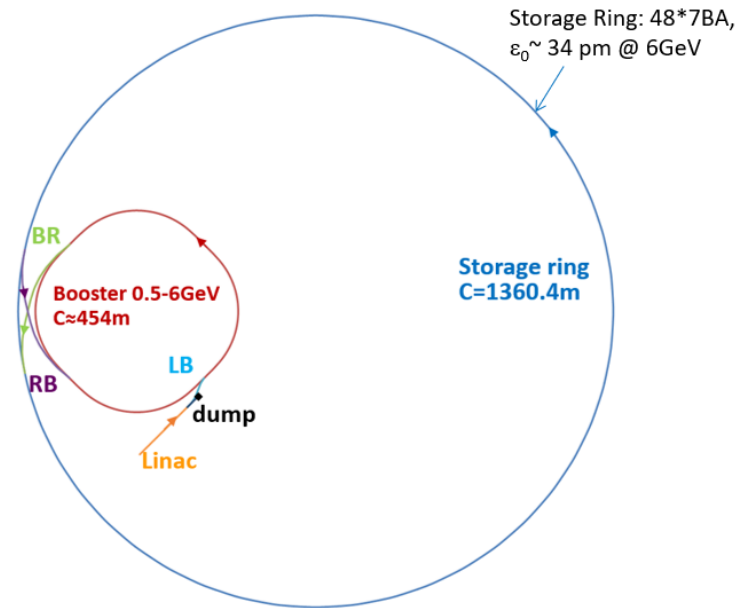
- 1. The HEPS Storage Ring BPM requirement**
- 2. BPM electronics design of HEPS project**
- 3. BPM electronics upgrading work in BEPCII project**
- 4. The plan of Pilot Tone Hardware used in HEPS**
- 5. Summary and Acknowledgement**

# **1. The HEPS Storage Ring BPM requirement**

# A quick introduction to the HEPS project

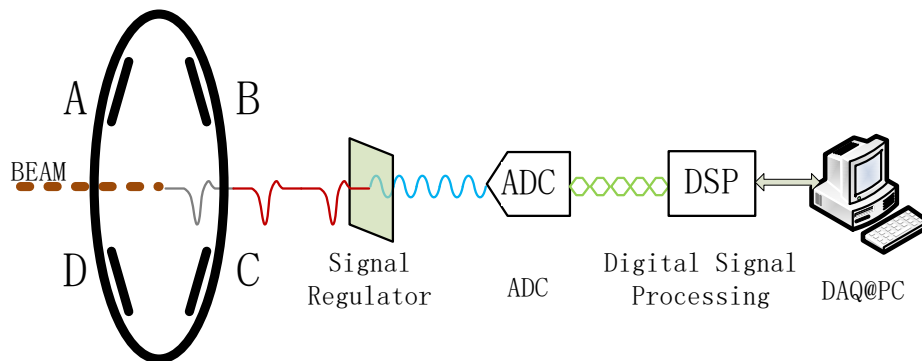
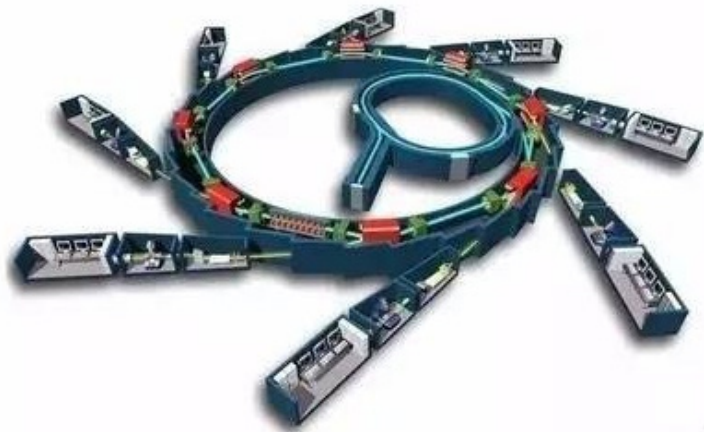
- The **High Energy Photon Source (HEPS)** is designed as an ultra-low emittance ring-based synchrotron radiation light ;
- About fourteen beamlines will be constructed in Phase I of the project;

- Storage ring circumference: 1360m, 48\*7BA
- Energy: 6GeV
- Emittance: 60pm.rad
- Current: >200mA



Schematic of HEPS Complex

# The Digital BPM requirement of HEPS project



## HEPS BPM quantities

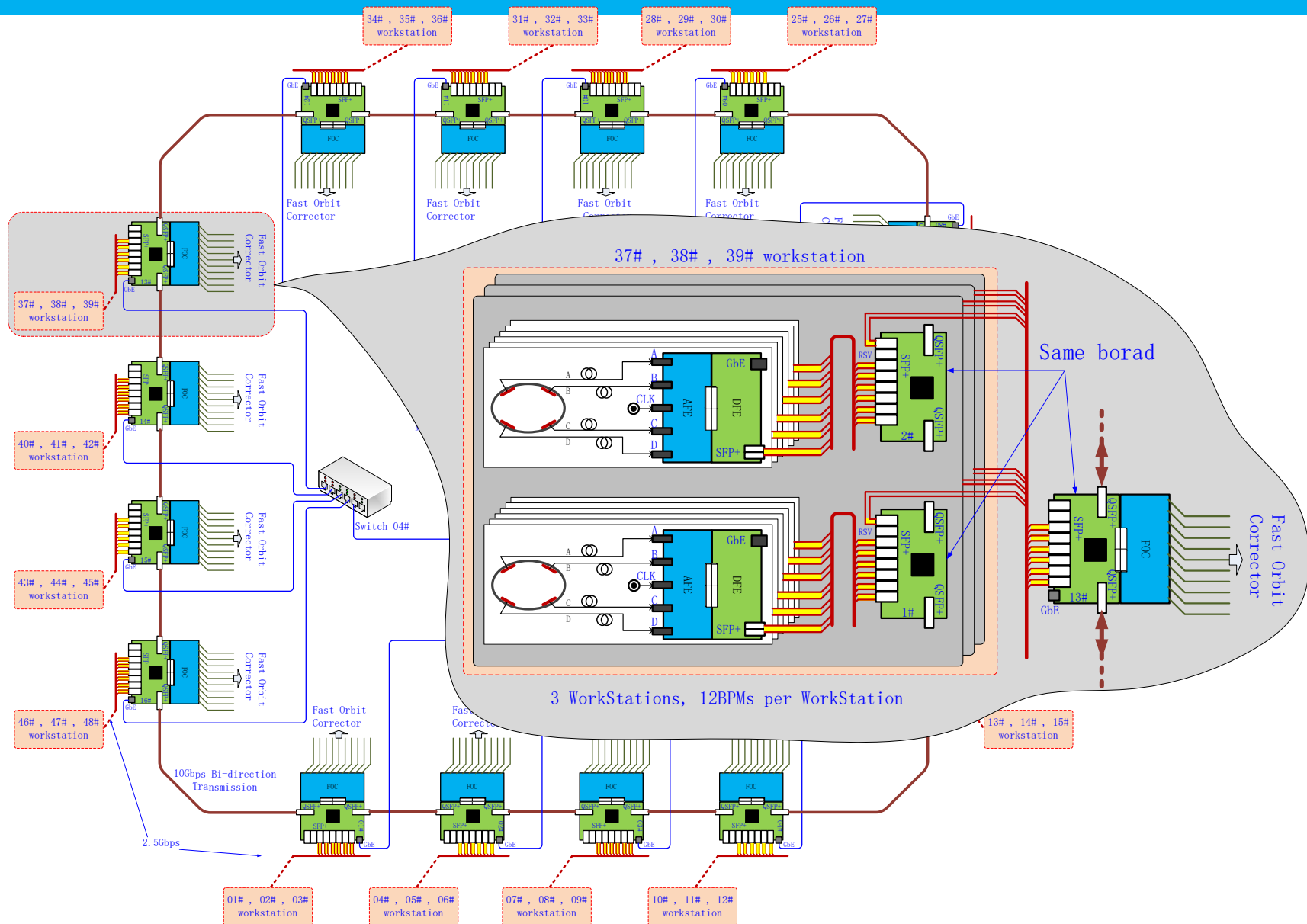
|               | BPM Quantities |
|---------------|----------------|
| Linac         | 7              |
| Transfer Line | 3*10=30        |
| Booster       | 80             |
| Storage Ring  | 48*12+2=578    |
| SUM           | 695            |

## Storage ring BPM Parameters

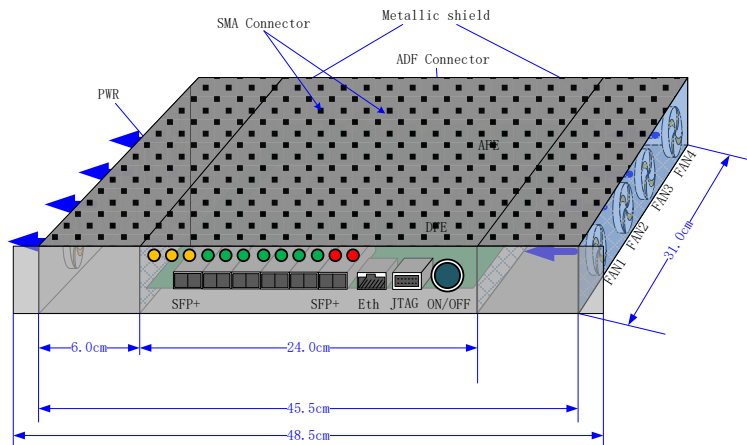
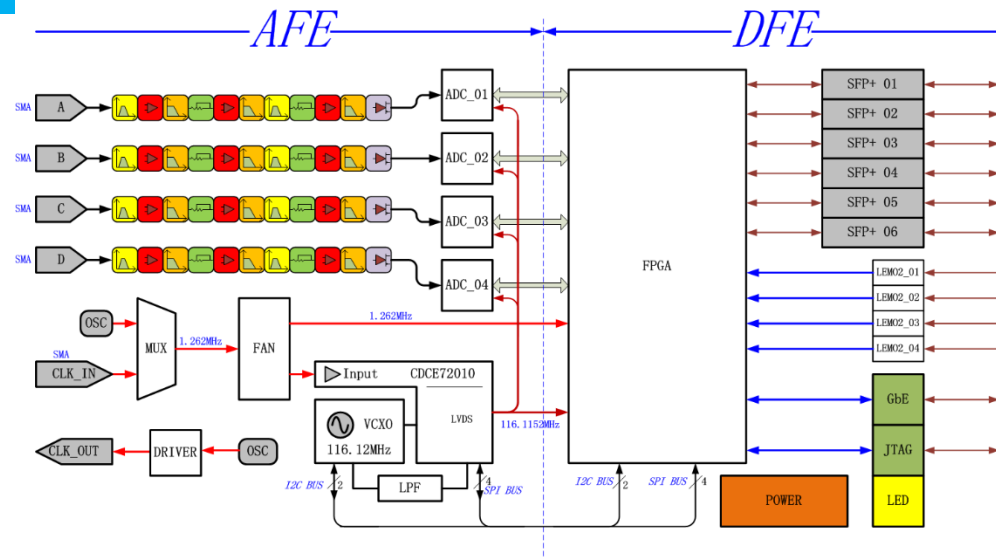
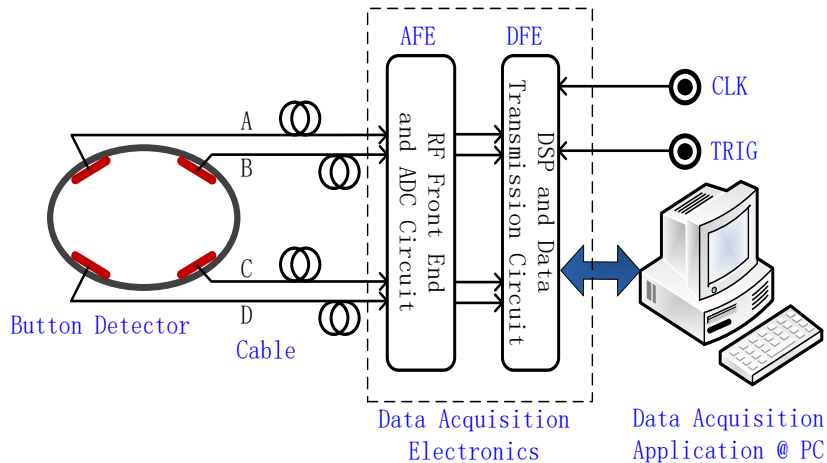
|                   | DBPM@HEPS           |
|-------------------|---------------------|
| Turn by Turn Data | <u>1μm @220kHz</u>  |
| FA data           | <u>0.3μm @22KHz</u> |
| COD data          | <u>0.1μm @10Hz</u>  |

## **2. BPM electronics design of HEPS project**

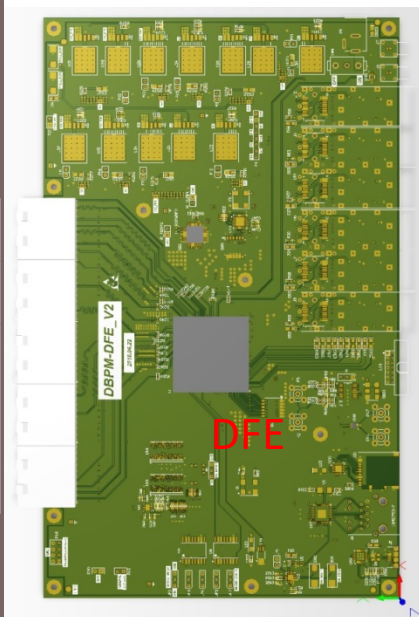
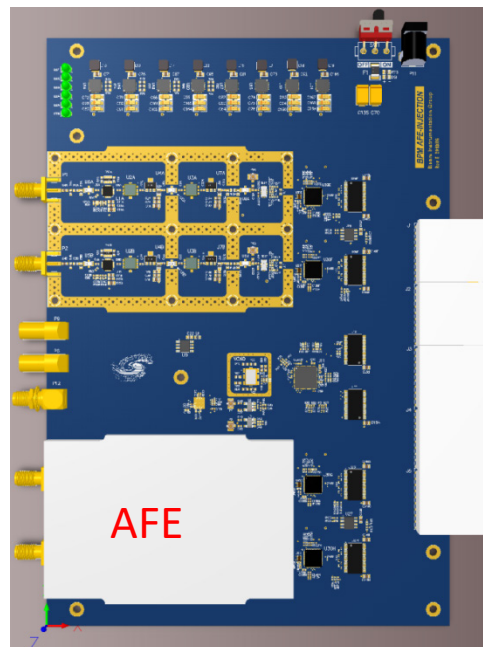
# 2.1 FOFB Framework and DBPM architecture



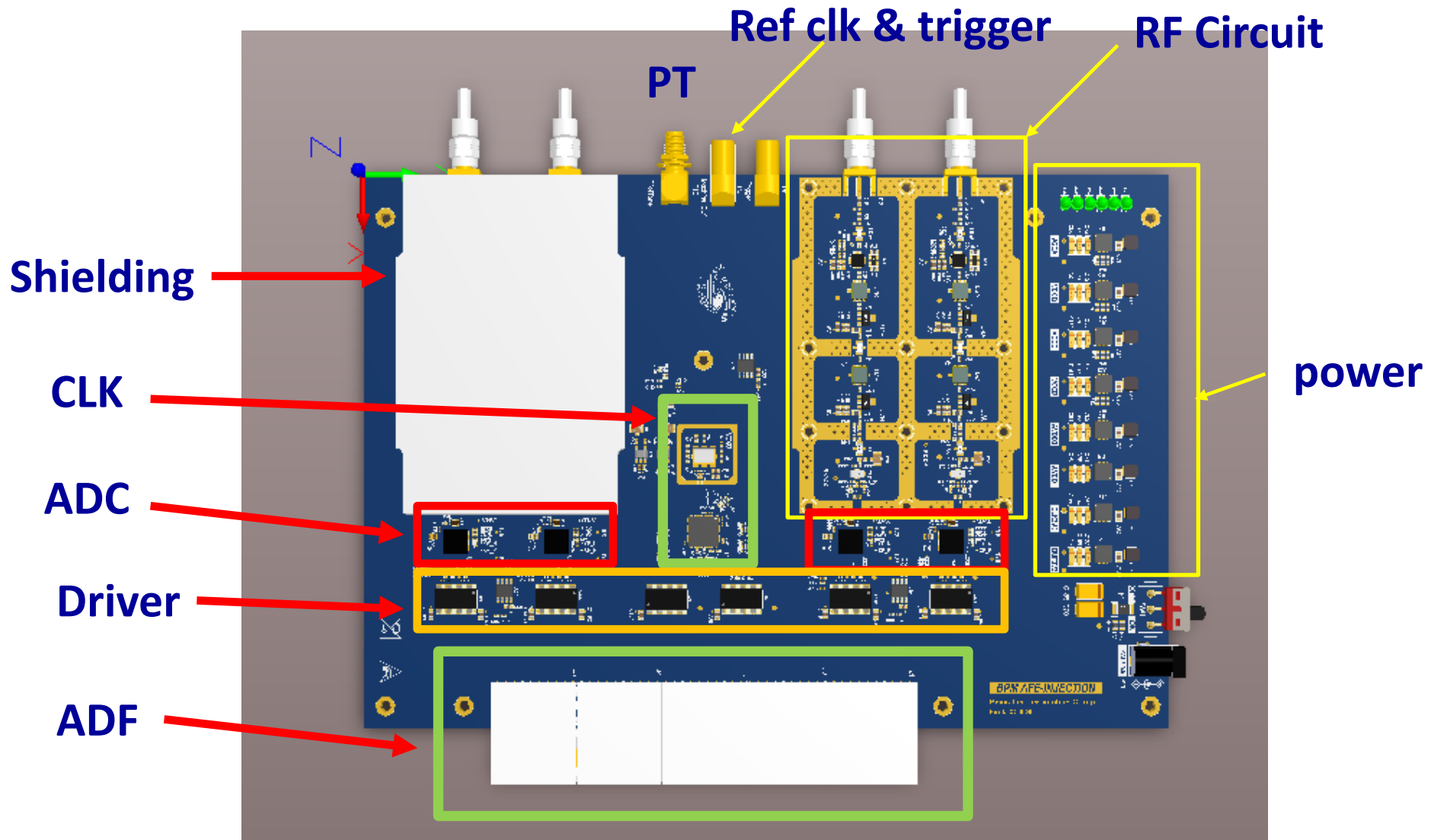
# 2.2 DBPM Electronics design



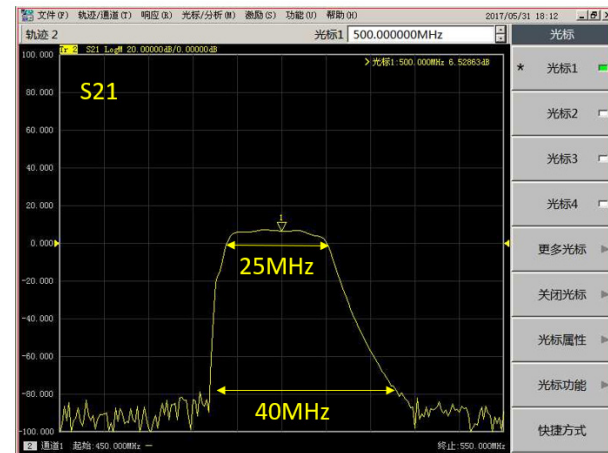
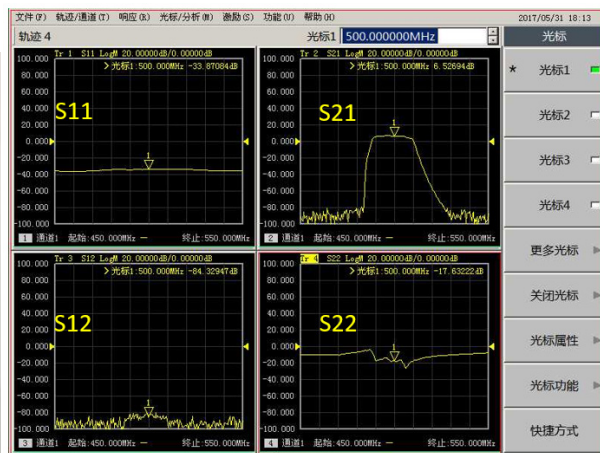
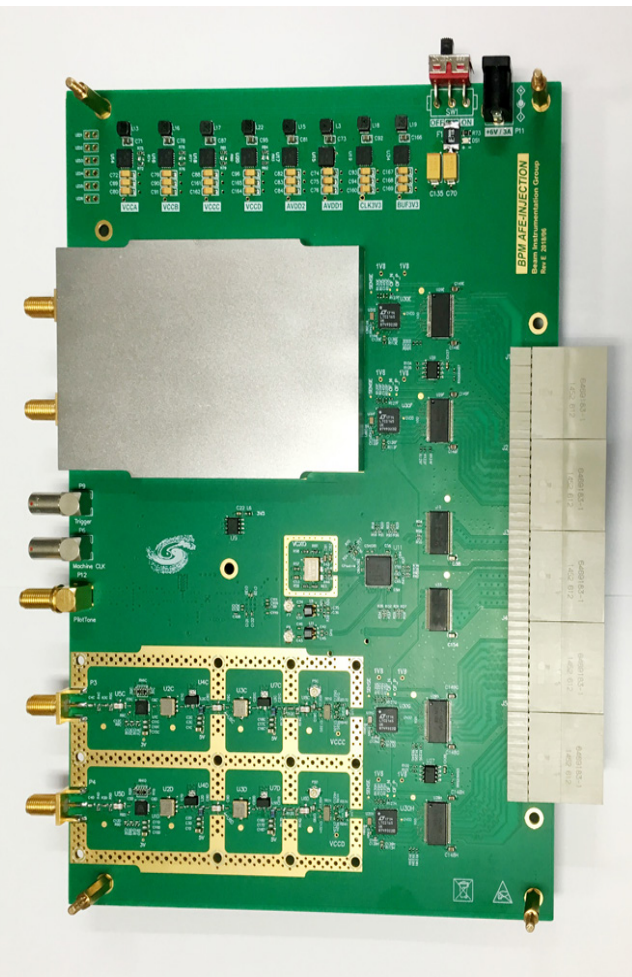
(By HuiZhou Ma)



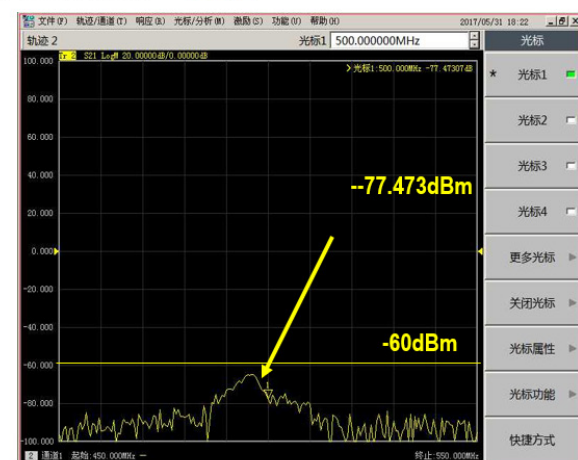
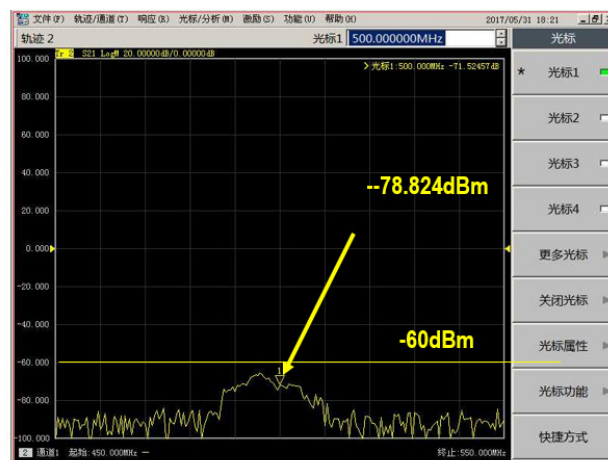
# ■ AFE electronic Design



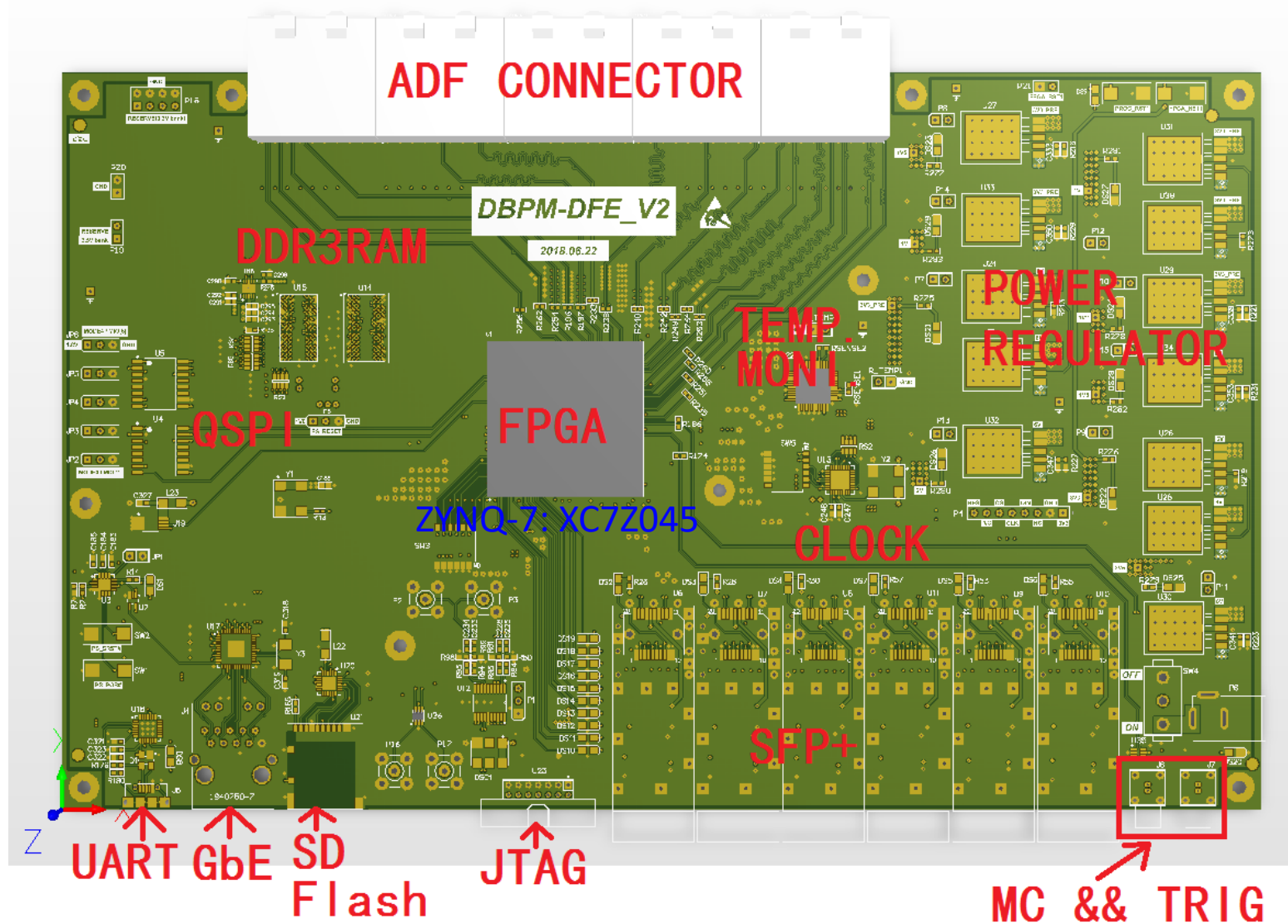
# AFE Analog logic Testing



Channel to Channel Isolation > 60dB



# ■ DFE electronic Design

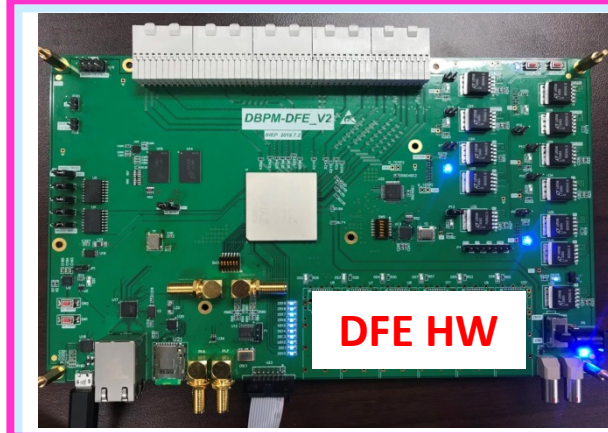
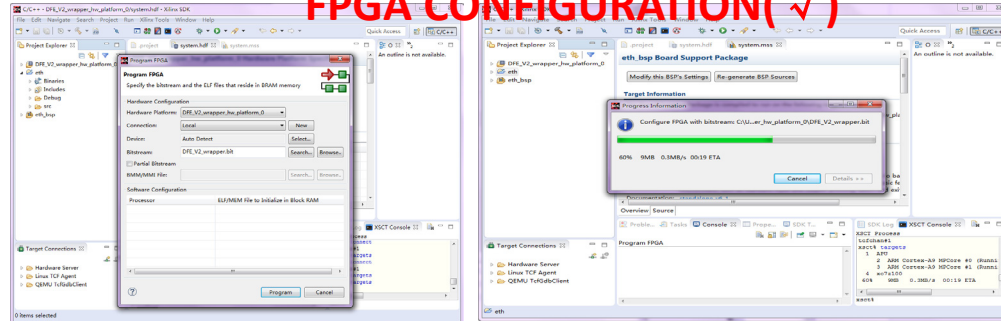


# DFE Hardware Testing

## DFE POWER(✓)

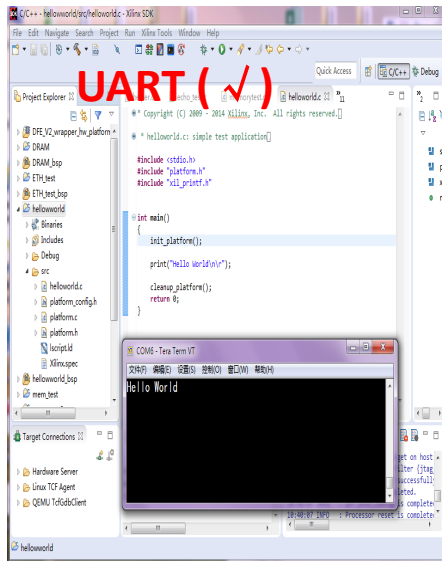
| 设计电压 (V) | 实测电压 (V) | 用电引脚                                                        |
|----------|----------|-------------------------------------------------------------|
| 1        | 1.006    | VCCINT, VCCPINT, VCCBRAM, ETH,                              |
| 1        | 1.003    | MGTAVCC                                                     |
| 1.2      | 1.213    | GTX_MGTAVTT                                                 |
| 1.5      | 1.494    | VCCO, DDR3                                                  |
| 1.8      | 1.780    | VCCPAUX, VCCPLL, VCCOMIO, VCCAUX, MGTAVCCAUX, UART, SD, I2C |
| 2        | 1.998    | VCCAUX_IO                                                   |
| 2.5      | 2.513    | VCCO                                                        |
| 3.3      | 3.315    | VCCO, ETH, JTAG, QSPI, POR,                                 |
| 3.3_pre  | 3.295    | 1.5V, 1.2V, 1V                                              |

## FPGA CONFIGURATION(✓)

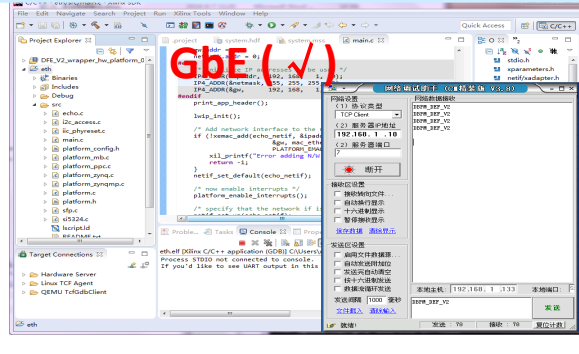


## DFE HW

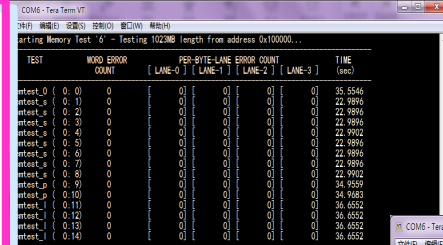
## UART(✓)



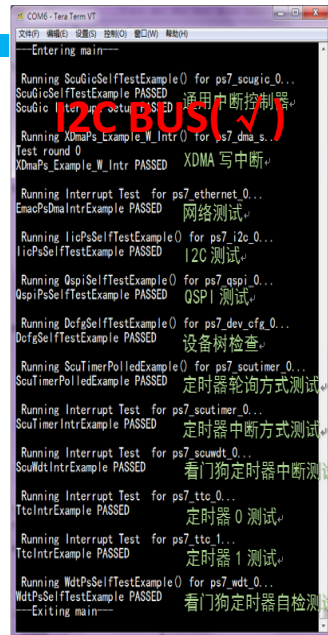
## GbE(✓)



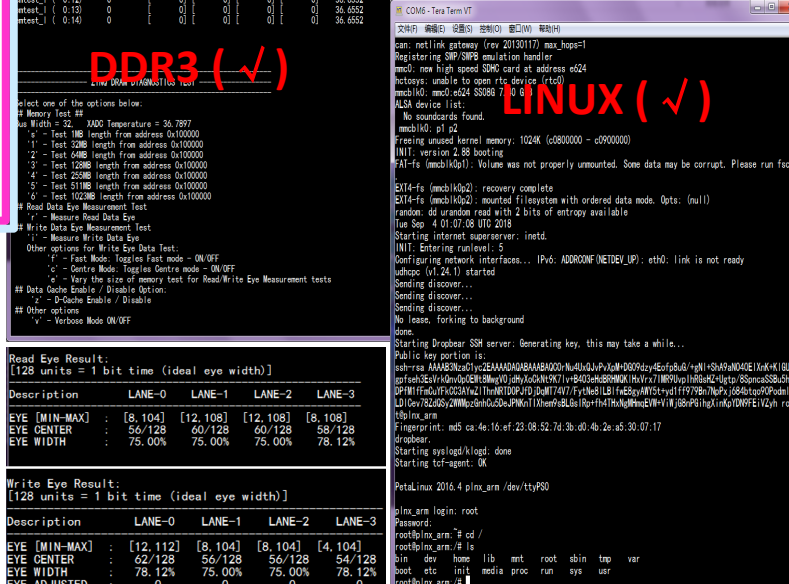
## DDR3(✓)



## I2C BUS(✓)



## LINUX(✓)



# 2.3 The HEPS BPM electronics Integration Testing

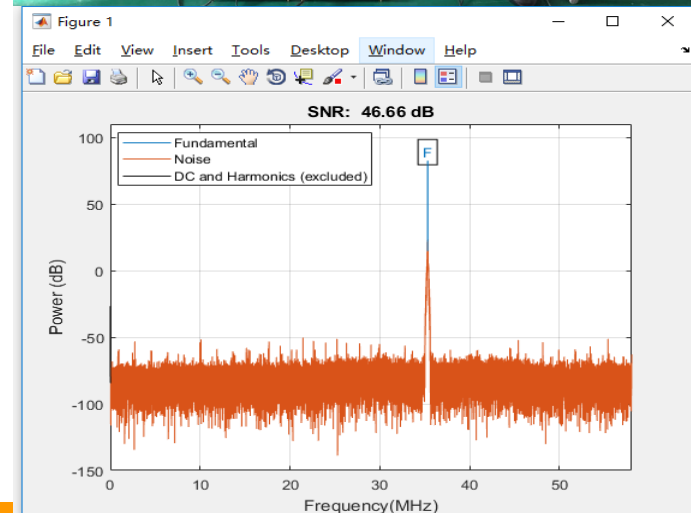
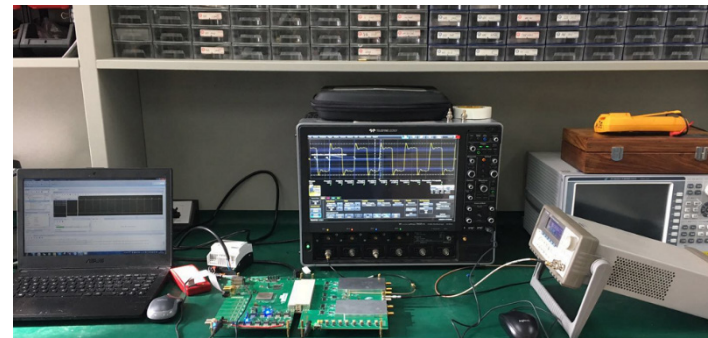
## ■ ADC Clock testing

- <1ps RMS Jitter

## ■ RAW Data testing in laboratory

- RAW data SNR: ~46.6dB
- Process (RAW data to TBT) gain from digital BPF: ~20dB

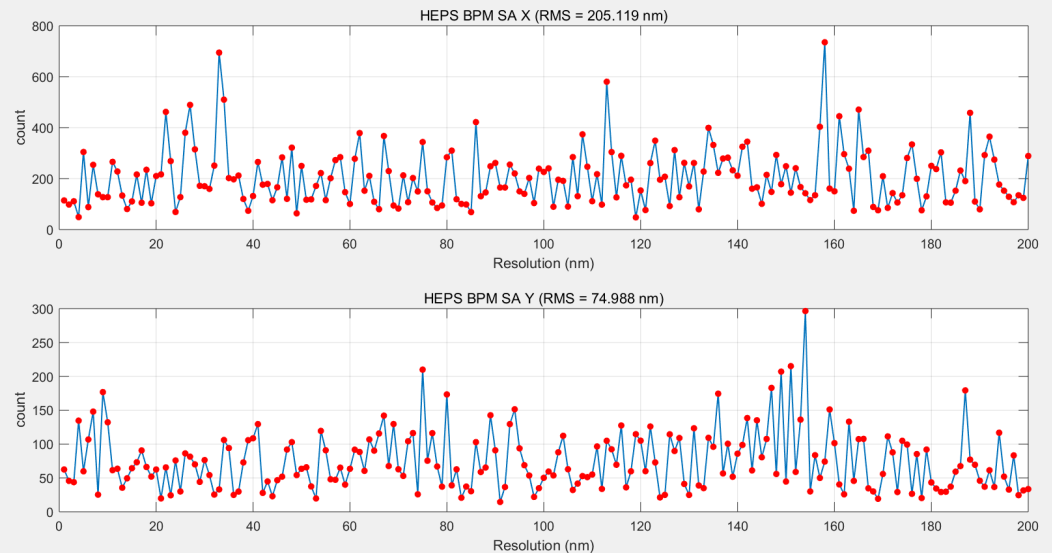
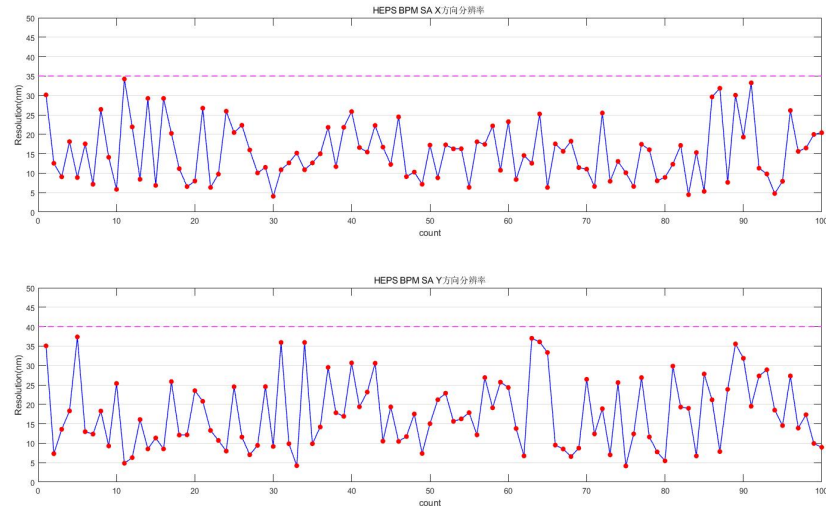
*\* FFT Process gain is not included!*



# The HEPS BPM electronics Performance Testing

SA data resolution  
STD testing  
( $K_x=K_y=8.26\text{mm}$ )

- Better than  
50nm@Laboratory
- Better than  
100nm@ BEPCII  
Real beam



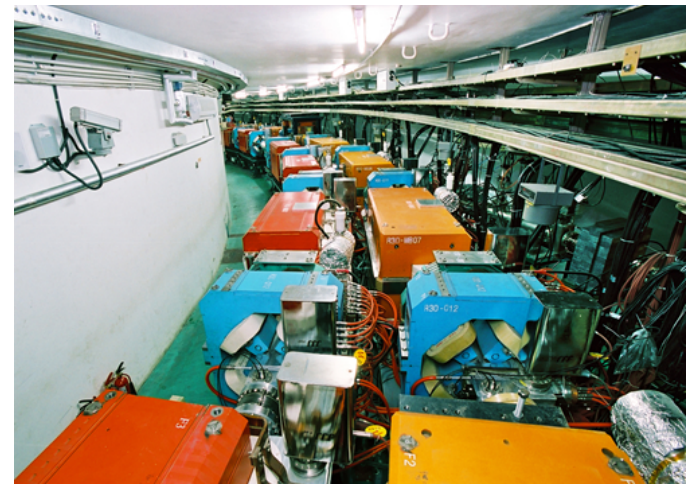
# **3. BPM electronics upgrading work in BEPCII project**

# **Why we do the BEPCII BPM electronics upgrading work, and why is it important.**

- The Bergoz BPM electronics in BEPCII have been worked more than 10 years, some of them broke down now.
- The work can bring benefit to the HEPS' BPM building.
  - The main function and performance of HEPS' BPM electronics can be proofed.
  - Any design flaws in BPM electronics can be found and solved during BEPCII BPM upgrading job.
  - The long-term stability of BPM electronics will be examined.
  - The mass production capacity of BPM electronics will be verified.

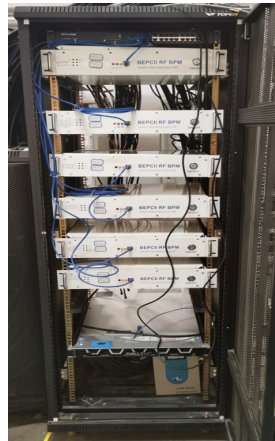
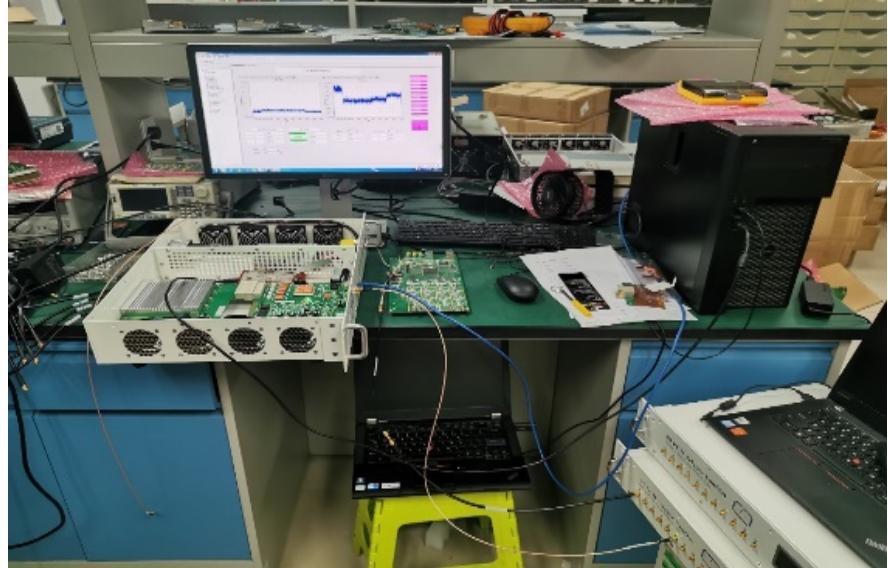
# What we have done and what we are about to be done in our upgrading job

- BEPCII Linac BPM electronics upgrading work have been finished in 2019.
- Storage Ring BPM electronics upgrading work of BEPCII will be completed in 2021

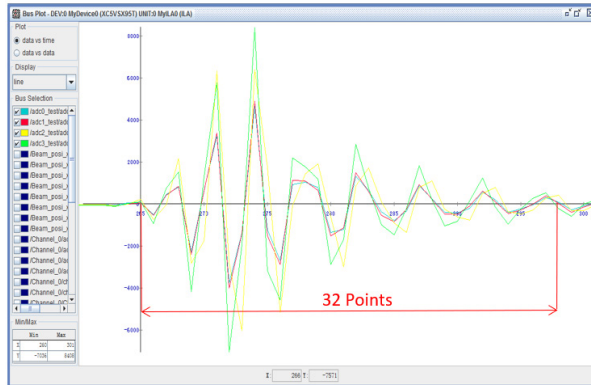


# BEPCII Linac BPM electronics upgrading work

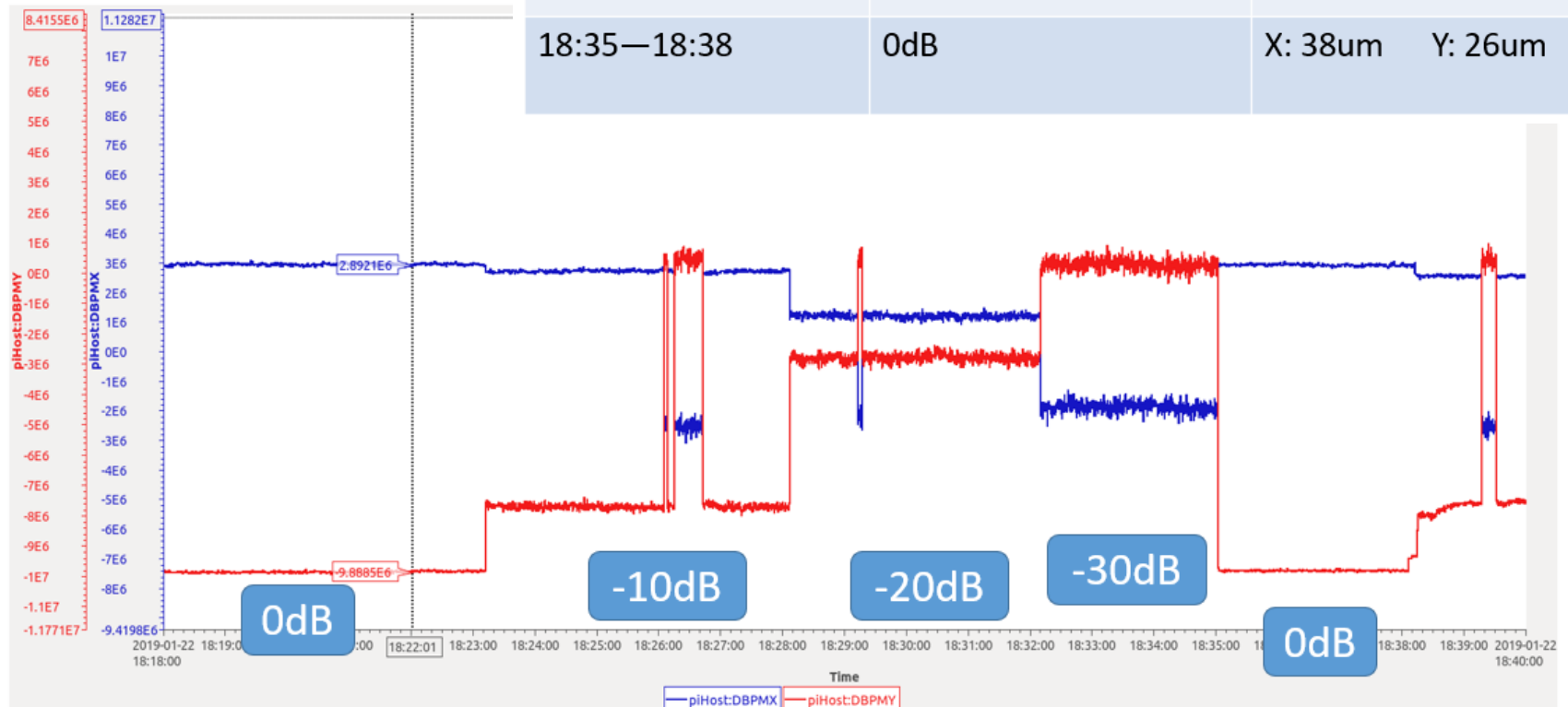
- About 20 Linac BPM electronics upgrading were completed in 2019



# Resolution testing with real beam in BEPCII LINAC



| TIME        | ATTENUATION SETTING | RESOLUTION |          |
|-------------|---------------------|------------|----------|
| 18:18—18:23 | 0dB                 | X: 38um    | Y: 26um  |
| 18:23—18:28 | -10dB               | X: 55um    | Y: 40um  |
| 18:28—18:32 | -20dB               | X: 85um    | Y: 70um  |
| 18:32—18:35 | -30dB               | X: 120um   | Y: 100um |
| 18:35—18:38 | 0dB                 | X: 38um    | Y: 26um  |

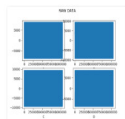


# BEPCII SR BPM electronics upgrading work

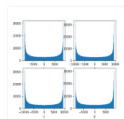
- All BEPCII Storage Ring BPM electronics will be upgraded within 2 years. Half of the total, about 50 BPM electronics, will complete the installation in 2020. And the rest will be installed in 2021.



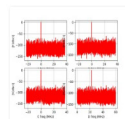
15.txt



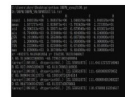
Figure\_1.png



Figure\_2.png



Figure\_3.png

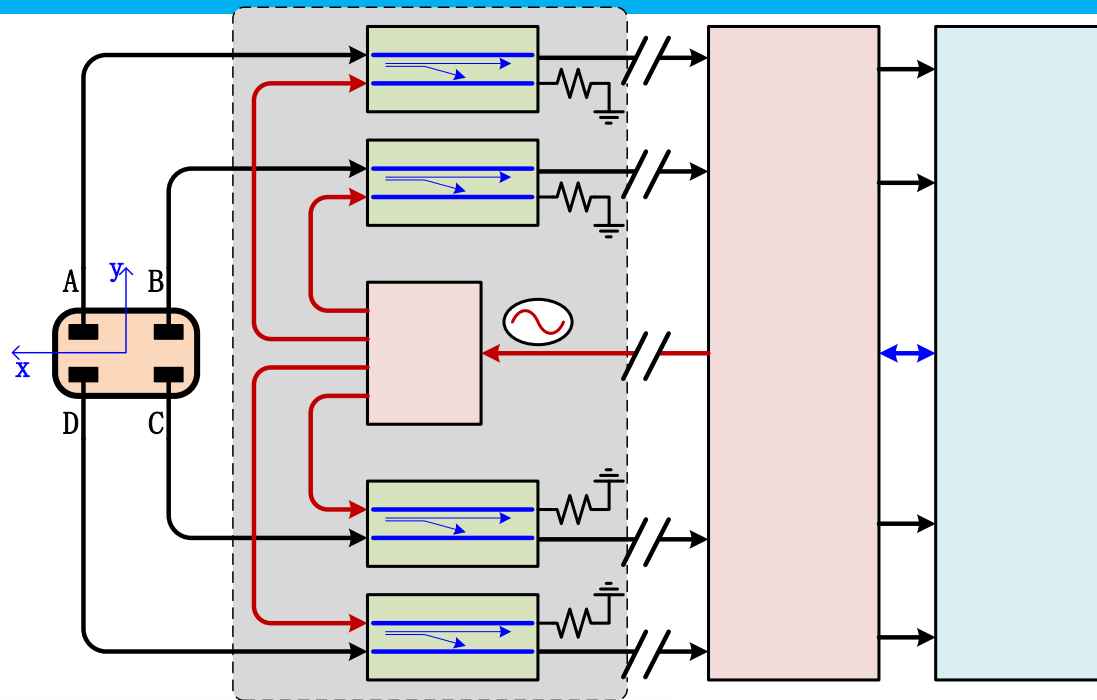


捕获.PNG



## **4. The plan of Pilot Tone HW used in HEPS**

# Pilot-Tone scheme and hardware

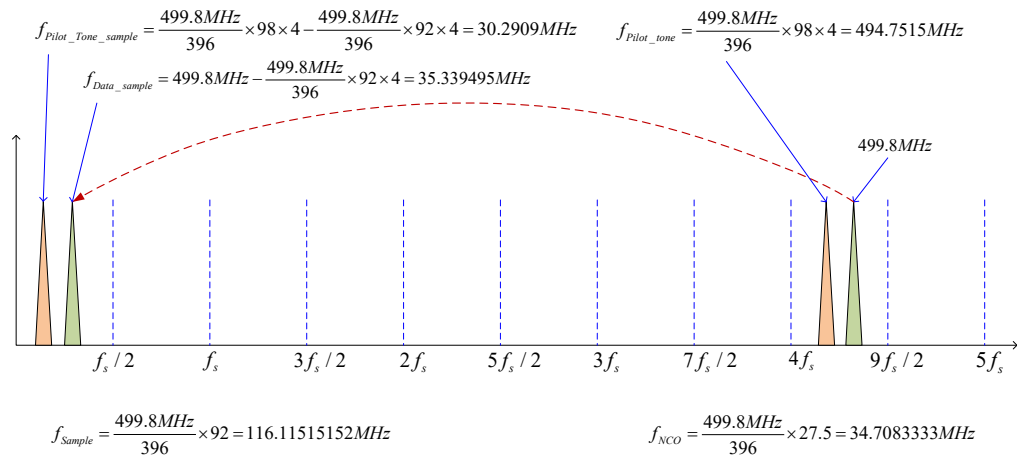


$$V_A = \frac{V_{A(BPM\_Signal)}}{K \times V_{A(Pilot\_Tone)}}$$

.....

$$X = K_X \times \frac{(V_A + V_D) - (V_B + V_C)}{V_A + V_B + V_C + V_D} + X_{offset}$$

$$Y = K_Y \times \frac{(V_A + V_B) - (V_C + V_D)}{V_A + V_B + V_C + V_D} + Y_{offset}$$

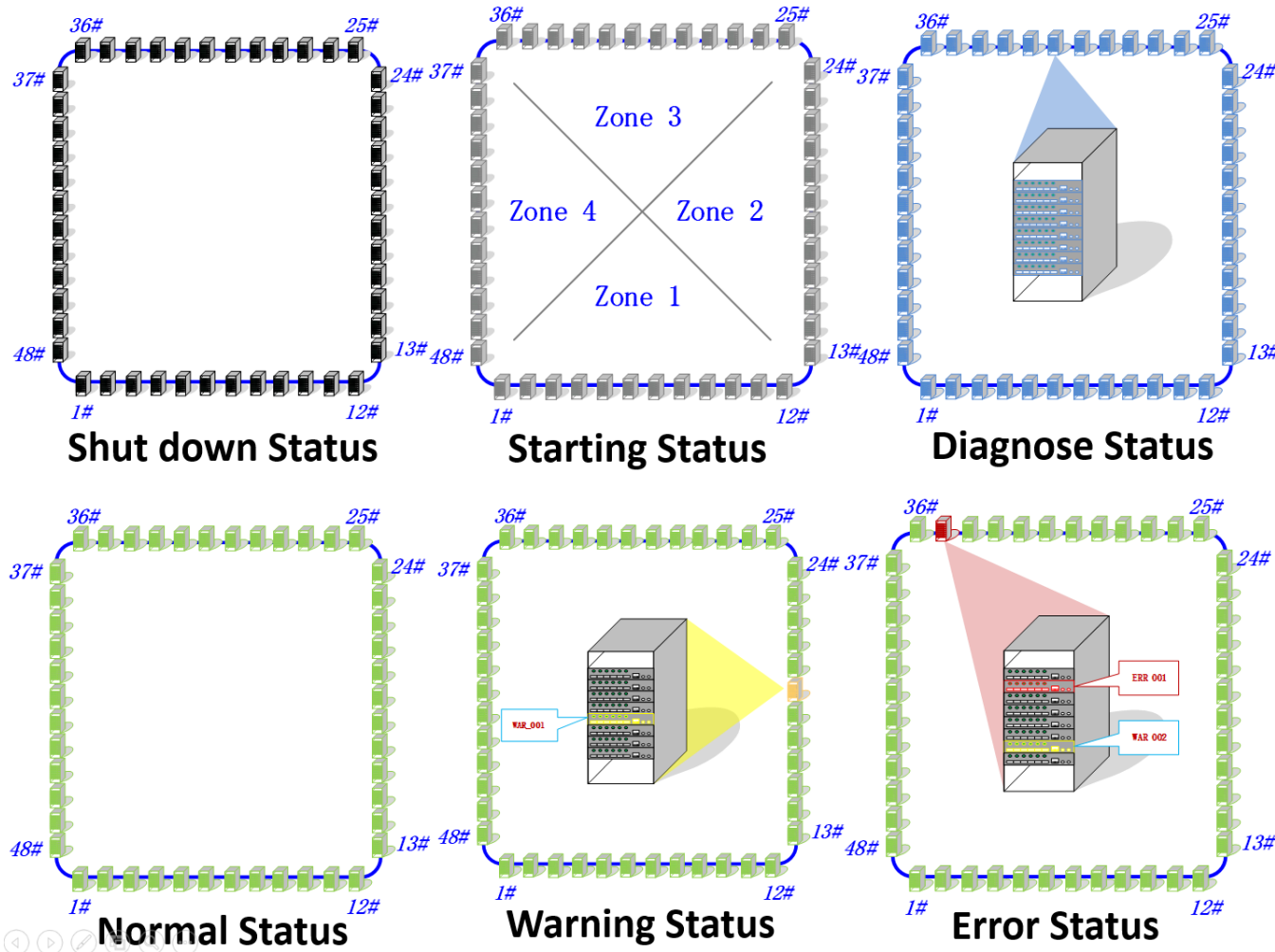


# The expected functions of Pilot tone logic in HEPS project.

- BPM **system self-testing** without beam.
- BPM electronics channels **on-line calibration**.
- BPM electronics **on-line diagnosis**.
- *The **on-line correction measurement** is our long-term target.*

# Prospective monitor interface in workstation

- Different colors for different operating states



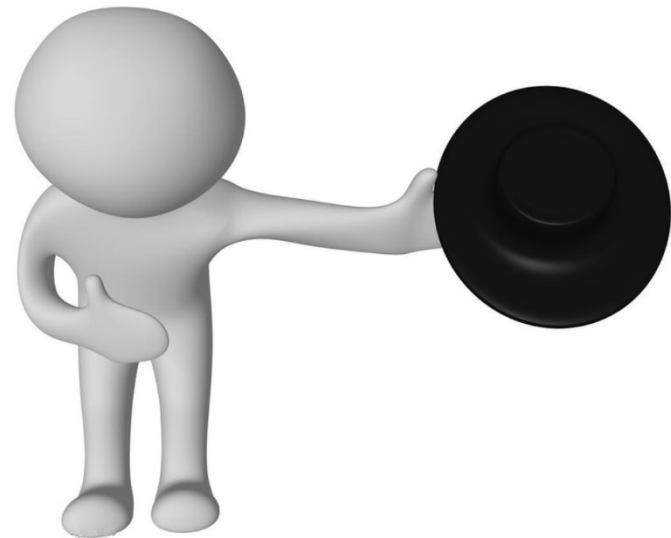
## **5. Summary and Acknowledgement**

# Summary

- Digital BPM Electronics hardware and algorithm has been designed carefully and had been tested in laboratory;
- The digital BPM electronics have been tested with the real beam on BEPCII.
- The digital BPM electronics have been used to replace the BEPCII's old Bergoz BPM electronics.
- Pilot Tone hardware will be built in HEPS project and used in special purpose.

# Acknowledgement

- During our Digital BPM electronic development, we got many experts help, and I would like to take this opportunity to express my sincere appreciation to those experts.
  - SIRIUS
  - SSRF
  - HLS
  - I-Tech
  - ...



***Thanks for your attention***