WEPP16

Advanced Light Source High Speed Digitizer*

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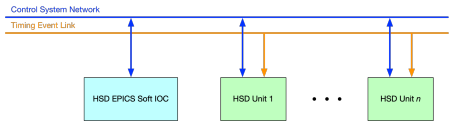
Abstract

The Advanced Light Source (ALS) is developing the High Speed Digitizer (HSD), a data acquisition system based on the latest Radio Frequency System-on-Chip (RFSoC) technology. The system includes 8 channels of 4GHz 4Gsps analog input, programmable gain, self-calibration, and flexible data processing in firmware. The initial motivation for the HSD project was to develop a replacement for aging ZTEC oscilloscopes that would be more tightly integrated with the ALS Control System and Timing System than any available commercial oscilloscope. However, a general approach to the design makes the HSD system useful for other applications, including a Bunch Current Monitor, as well as for other facilities beyond ALS.

Architecture

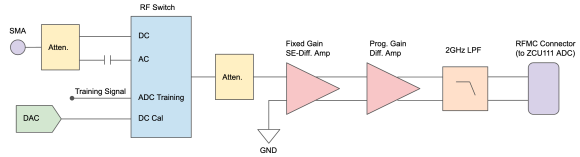
The HSD system architecture is consistent with the network-attached device (NAD) model used for ALS in-house designed instrumentation systems, as shown in Fig. 1. The architecture is flexible in that the number of soft IOCs required to support devices and how they are connected can be adjusted to trade off network bandwidth, CPU performance, and maintenance complexity. In the case of ALS, the small number of HSD units and low average data transfer rate make it suitable for a single soft IOC. Each HSD unit communicates with the EPICS soft IOC via a clean and simple UDP interface, which allows either side to be upgraded independently. Each unit also receives the timing event link from the timing distribution infrastructure.

The HSD design is intended to be general purpose to accommodate multiple applications, including as a Fast Scope and Bunch Current Monitor, and others that fit the specifications. The firmware can be modified to achieve this with the same hardware configuration.



Conclusion

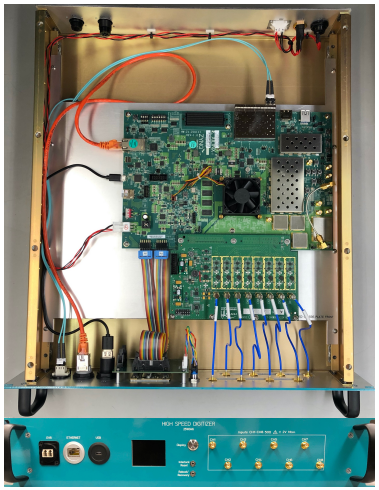
The High Speed Digitizer meets the performance goals for both ALS and ALS-U as both a fast oscilloscope and Bunch Current Monitor, and shows promise for addition-al applications and accelerators. Features such as 8 chan-nels, tight integration with the timing system for trigger-ing and RF-synchronous sampling, and flexible firmware, along with lower cost per channel are advantages over equivalent commercial oscilloscope products. With low quantities and low average data rates, the network-attached device architecture is a good fit for the EPICS control system at ALS and ALS-U.



Hardware

The HSDAFE has identical front end circuits for each of the 8 analog inputs, as shown in Fig. 3. The maximum analog input level is ±2 V (+16 dBm) and is protected from overvoltage by a dual Schottky barrier diode. The input signal is then attenuated by 6 dB. An RF MEMS SP4T switch selects between four input paths: DC-coupled, AC-coupled, DC calibration, or ADC training. To simplify the design, calibration and training signals are shared across all channels, so only one channel can be calibrated or trained at a time. The training signal is a digital output from the ZCU111 connected through a passive RC low pass filter into the RF switch.

A 15 dB attenuator scales the maximum signal amplitude to the fixed gain amplifier input range. A programmable gain amplifier is scaled so a full scale input signal at the SMA connector drives the RFSoC ADC full scale at a gain of +6 dB, where the maximum gain is +26 dB, providing 20 dB of usable programmable gain range in 1 dB steps. A simple differential RC low pass filter at 2 GHz provides anti-aliasing at the ADC input. A single capacitor can be replaced with a different value to change the filter bandwidth, or removed to drive the ADC unfiltered.

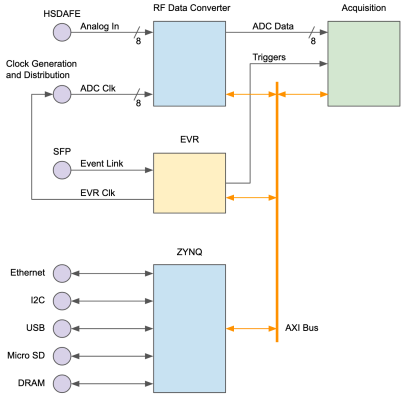


Firmware

For the FS application, the ADC sampling clock runs at fRF*8 (~4 GHz). The Acquisition core supports flexible triggering from the EVR or self-trigger detection, and stores up to 64 k values for each channel in block RAM. Data can be acquired continuously or in segments of pro-grammable separation and length (i.e., for Booster TWE measurements of the same bunches at different times during the ~0.5 sec ramp). For the BCM application, the ADC sampling clock runs at fRF*80/11 (~3.6 GHz). The Acquisition core computes and stores a sum at each point over a 'turn', which is multiple actual turns of the beam, with interleaved sampling similar to a sampling oscillo-scope.

For both applications, the rest of the firmware is the same. The EVR core decodes the recovered RF EVR clock and timing events from the event link. The EVR clock is sent off-chip to a clock generation and distribution circuit to generate the ADC sampling clocks. The EVR core con-tains trigger selection and control logic, and sends trig-gers to the Acquisition core. Analog inputs from the HSDAFE are connected to the ADCs in the RF Data Converter core. ADC parallel data is sent from the RF Data Converter to the Acquisition core, where it is trig-gered, processed, and stored as needed for the target appli-cation.

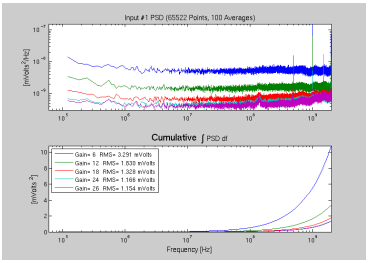
The ZYNQ core contains the embedded processor that runs the FPGA application. The FPGA firmware, boot-strap loader and executable image are stored in a single file on the micro SD card. This file can be uploaded to, or downloaded from, the card using the TFTP server in the FPGA application.



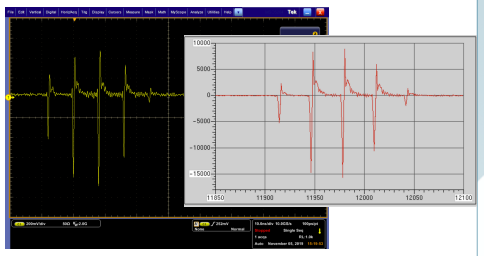
Status

The High Speed Digitizer production first article has been built and is planned to be installed at ALS in the next few months. The remaining ALS production units are being built, and will be installed later this year. ALS-U production units will be built when the project receives construction phase funding approval.

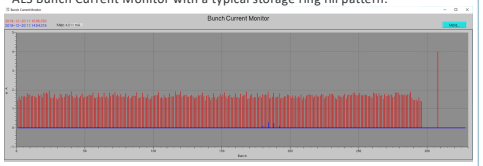
Power spectral density (PSD) and integrated PSD at different programmable gain settings with no signal on the input.



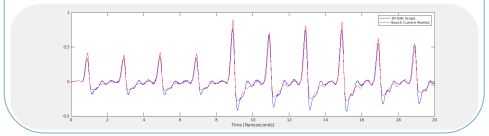
ALS Booster BPM button signal on a 2GHz Tektronix scope (left) vs. the HSD with a 1.3GHz low pass filter on the input.



ALS Bunch Current Monitor with a typical storage ring fill pattern.



ALS Bunch Current Monitor (red) vs. 30GHz Tektronix scope (blue).



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