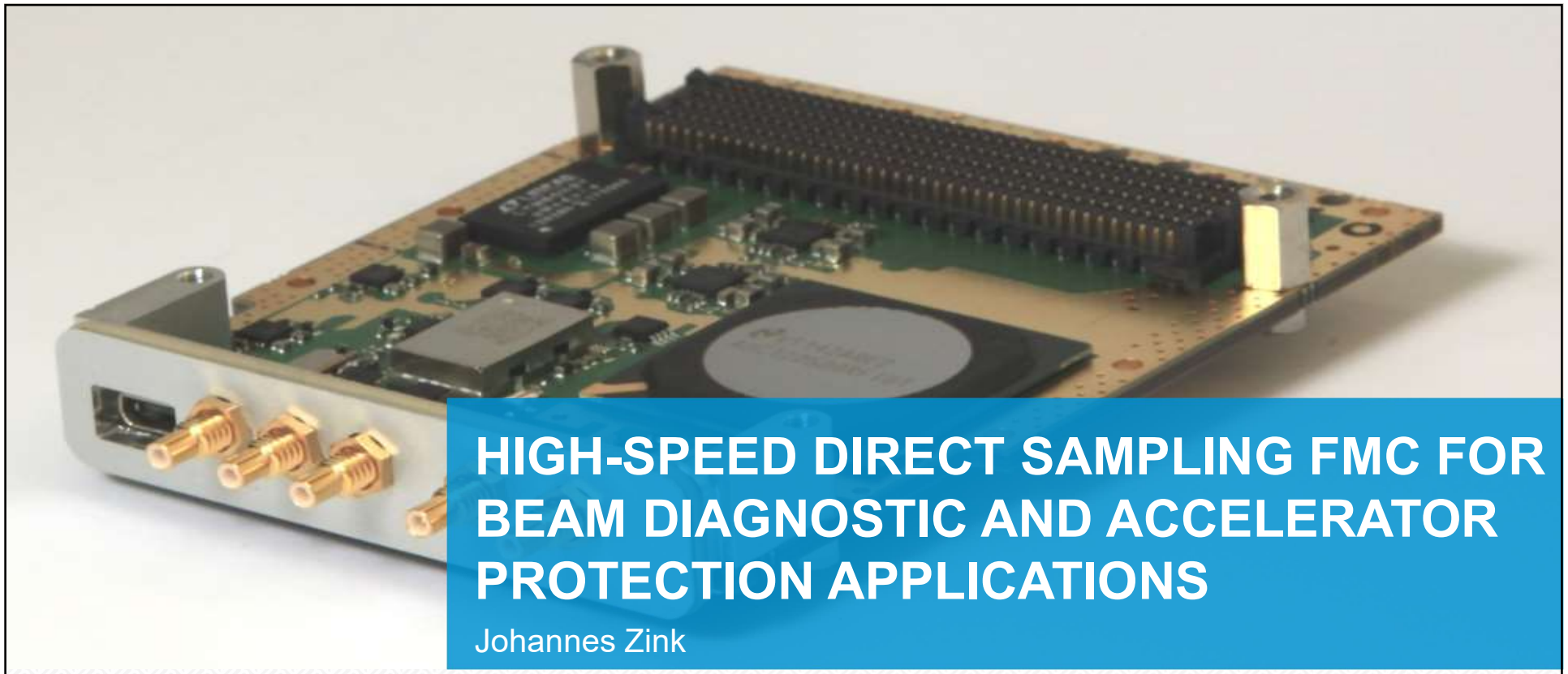


HIGH-SPEED DIRECT SAMPLING FMC FOR BEAM DIAGNOSTIC AND ACCELERATOR PROTECTION APPLICATIONS

Johannes Zink

MicroTCA TECHNOLOGY LAB

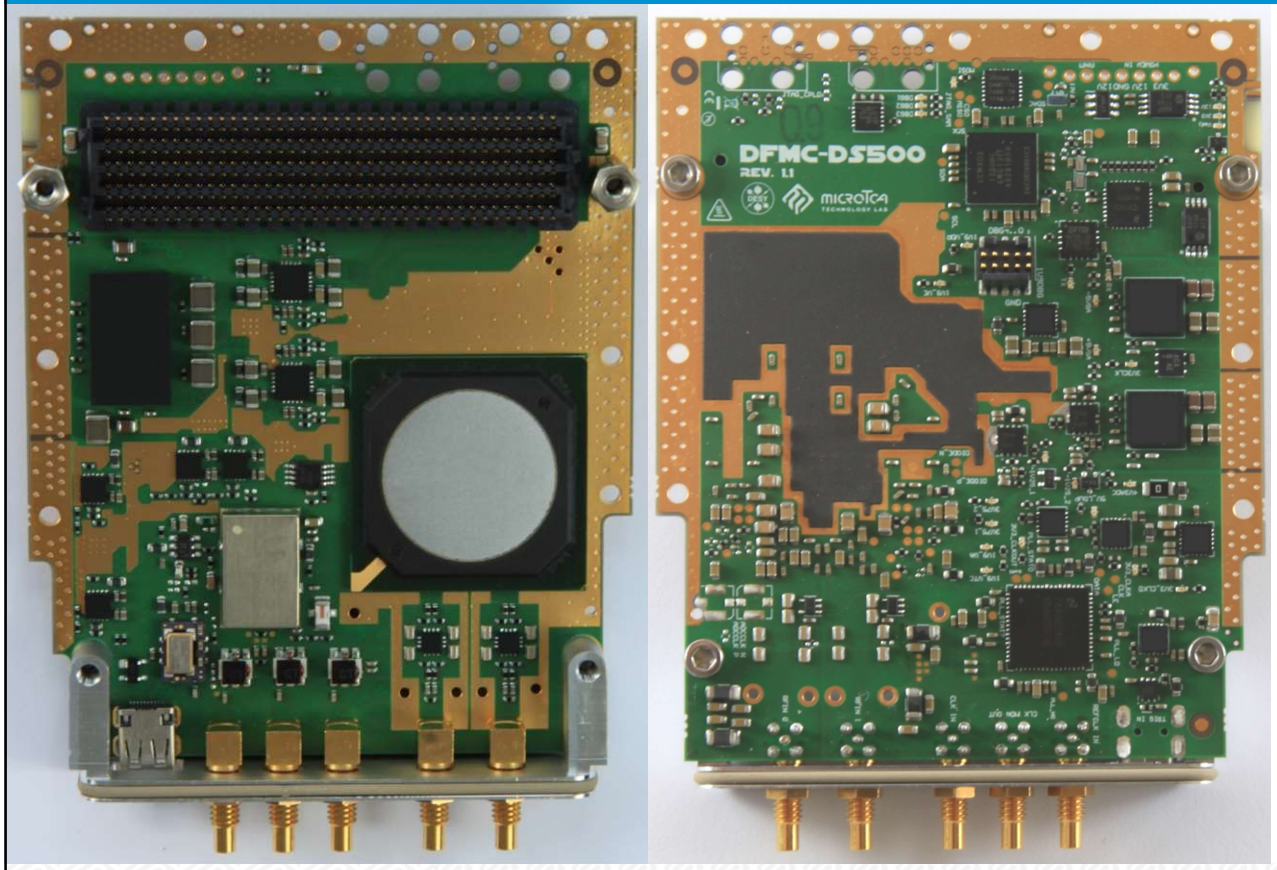
DESY.

7th IBIC, Shanghai 2018

AGENDA

1. DFMC-DS500 Digitizer Board
2. DAQ-System (Firmware / Software)
3. Coarse BAM Channel in FLASH
4. Test Measurements and Results

DFMC-DS500 Overview



- single width FMC according to ANSI/VITA 57.1 standard
- 8.5 mm stacking height
- air cooled, shielding cage + heatsink planned
- front panel: 5 RF SSMC + 1 HDMI Type D (micro) connectors
- 12-Bit, 500/800 MSP/s Dual Ch., 1/1.6 GSP/s Single Ch.

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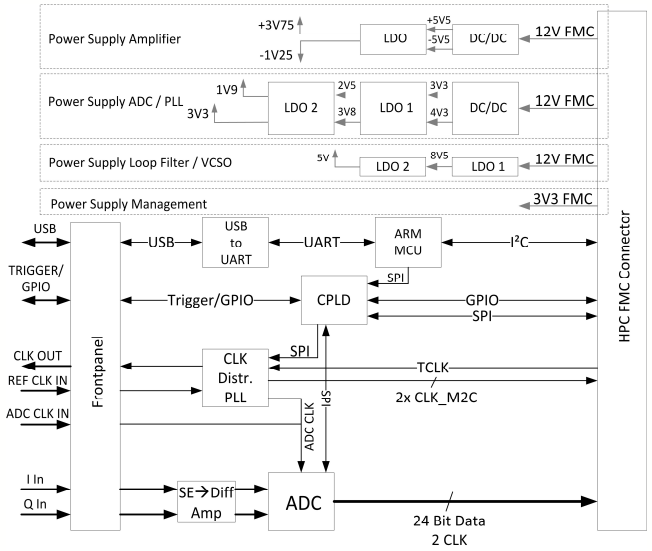
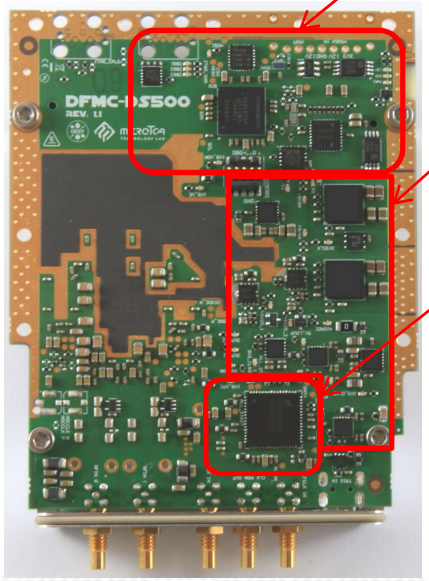
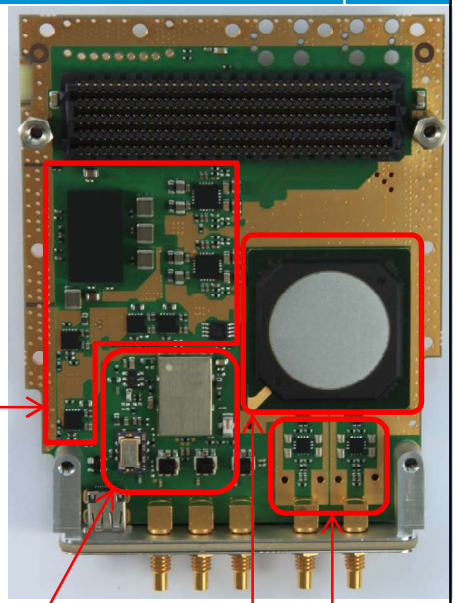
DFMC-DS500 Overview

- ADC input bandwidth: 2.7 GHz
- fully diff. amplifier [4,5] LS bandwidth: 4.8 GHz
- no anti-aliasing filter present
- variants with up to 3.2 GSP/s







Management

Power Supply

PLL

Oscillators/Loop Filters

ADC

SE → DIFF Amplifiers

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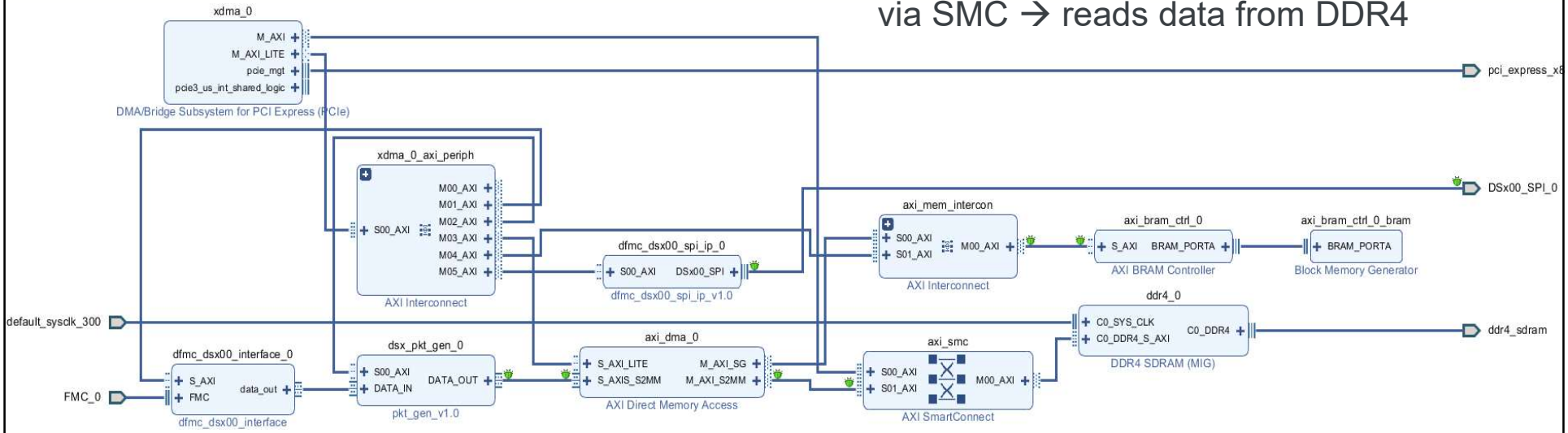
DAQ-FPGA

- DFMC-DSX00-INTERFACE connected to LVDS data lanes → delay calibration
- DSX_PKT_GEN generates AXI stream pakets readable by AXI DMA core

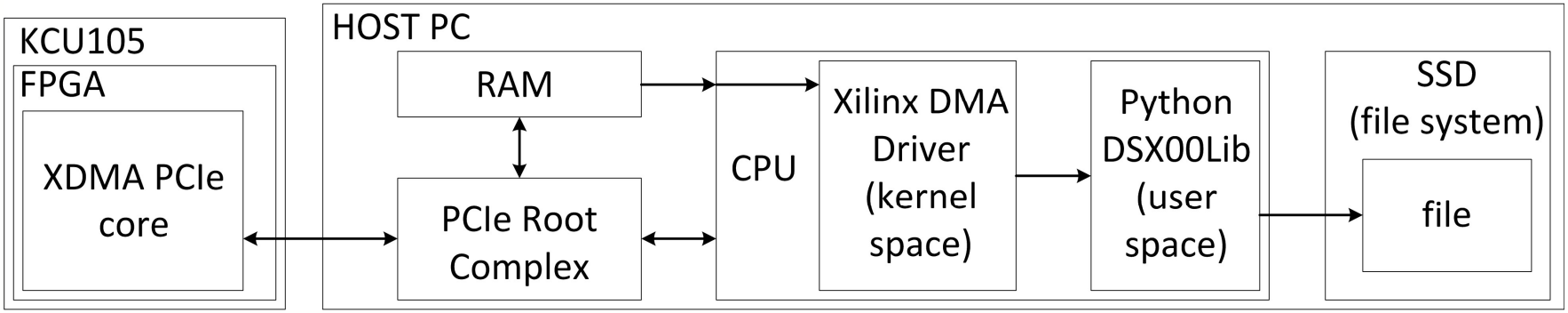
(see also THOA01, IBIC 2018, J.Marjanovic for data post-processing)

- AXI_DMA dumps data into DDR4 via AXI SmartConnect
- XDMA PCIe core controls cores via AXI Lite
- XDMA has full AXI connection to DDR4 via SMC → reads data from DDR4



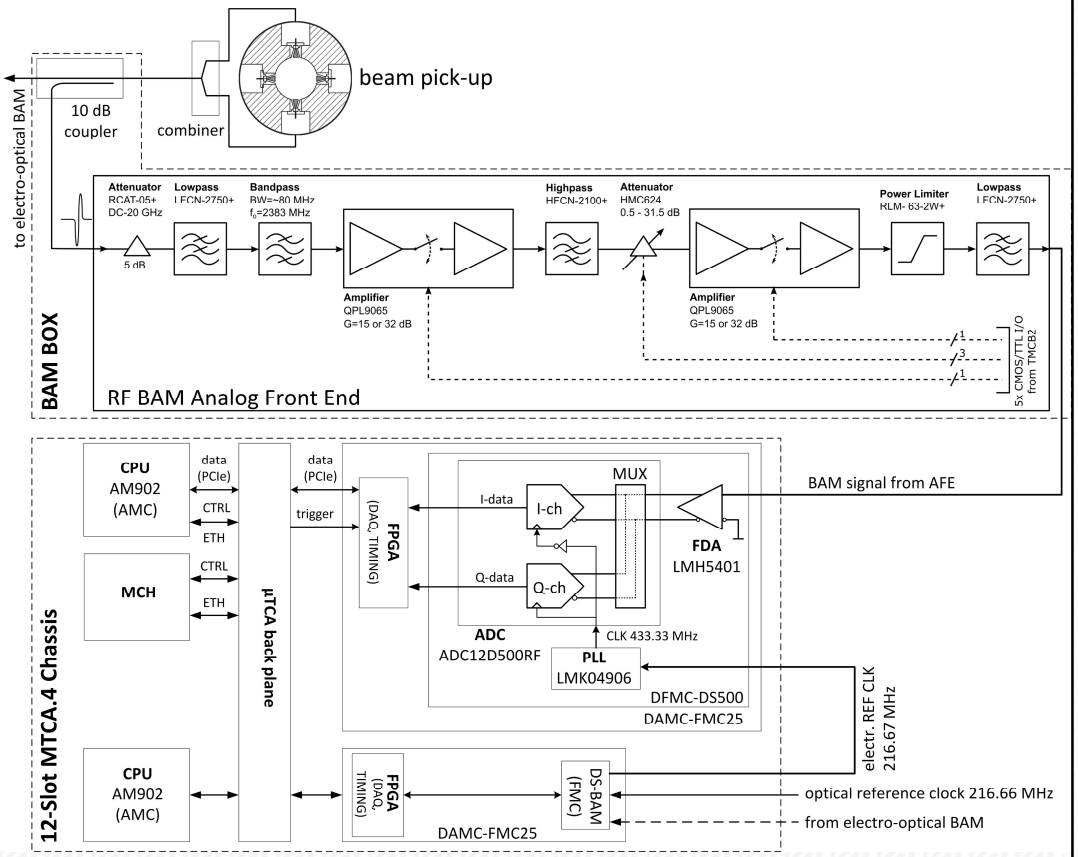
DAQ-Software

- straight forward solution for DAQ
- XDMA transfers sample data from DDR4 (KCU105) into host PC‘s RAM via PCIe root complex (DMA controller)
- Xilinx DMA driver (kernel space) provides pointer for DMA transfers into RAM
- Python library DSX00Lib can access transfered data in kernel space
- data can be dumped into file on SSD/HDD
- over 1 Mio. samples per channel can be stored on KCU105 (2GB DDR4)
- 8k samples can be stored on DAMC-FMC25 (256 MB DDR2)

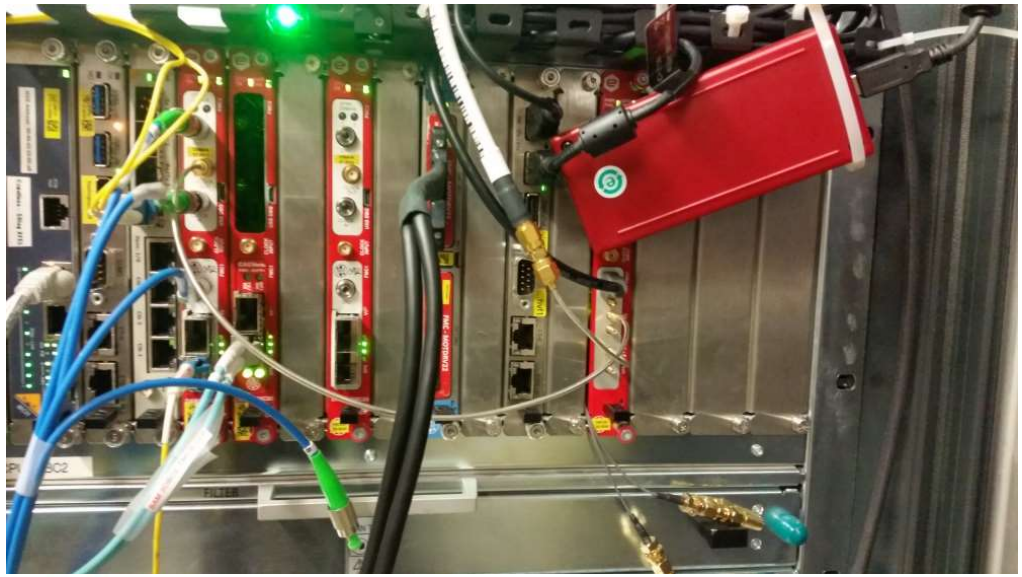


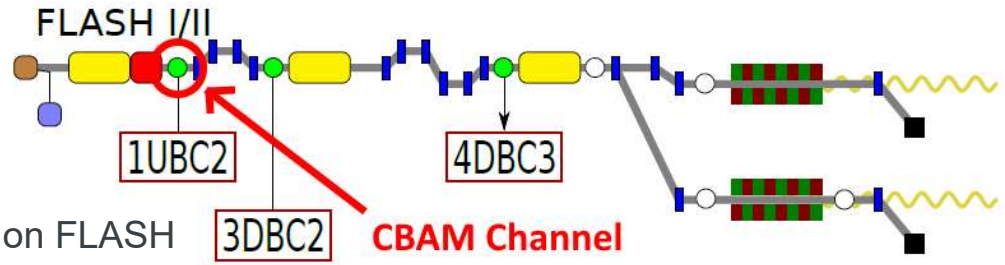
Coarse BAM Channel

- coarse BAM Channel planned in FLASH
- coarse BAM channel in addition to electro-optical BAM [1,2] → automatically adjust optical delay lines
- uses same combined high-bandwidth pick up [3] signals (40 GHz)
- analog front end bandpass filters the pick up signal
- bunch charges can vary from 20 pC up to 1 nC, which requires a dynamic range of about 34 dB
- sampling (DFMC-DS500/DAMC-FMC25) and processing in MTCA.4 crate



CBAM Channel in FLASH

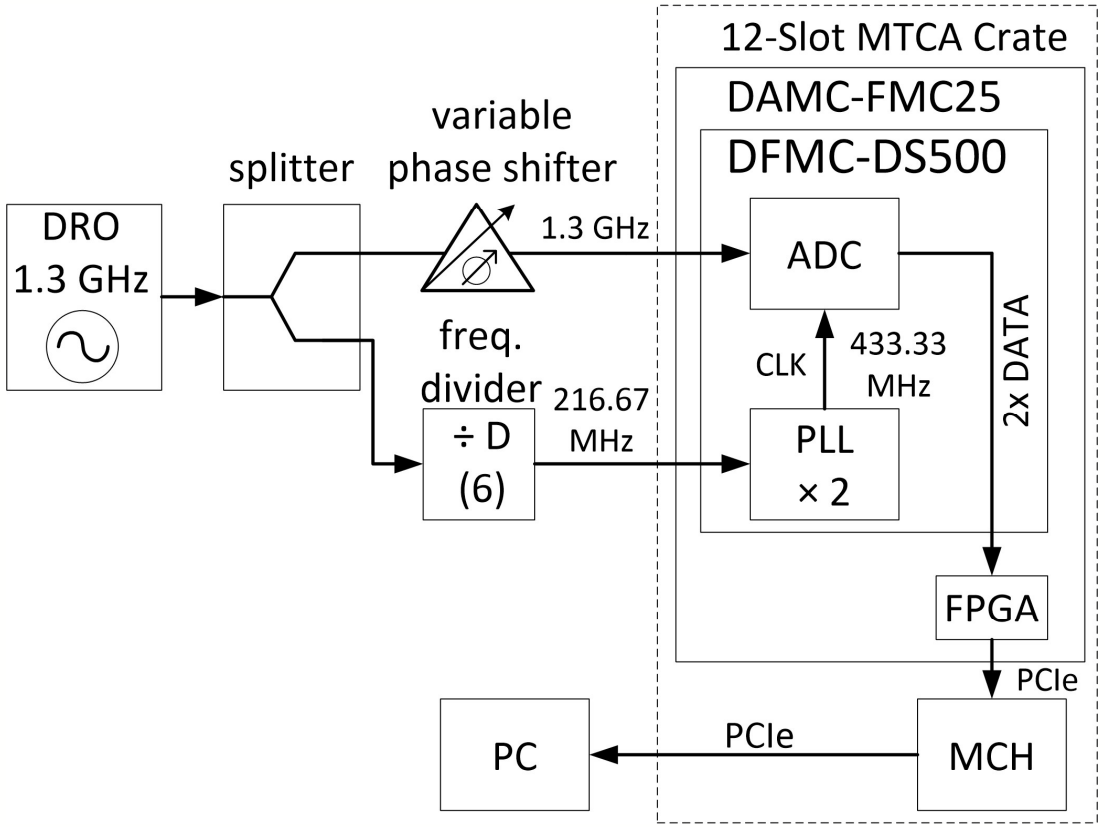




MOOB03, IBIC 2018, N. Baboi et al. for more details on FLASH

CBAM DS500 Test Setup

- complex high-bandwidth pick up signal
- testing ADC performance under ideal conditions with reduced signal bandwidth
- undersampling 1.3 GHz carrier with phase synchronous ADC clock → produces DC signal
- timing error converts into amplitude error
- roughly estimate the timing accuracy



Results

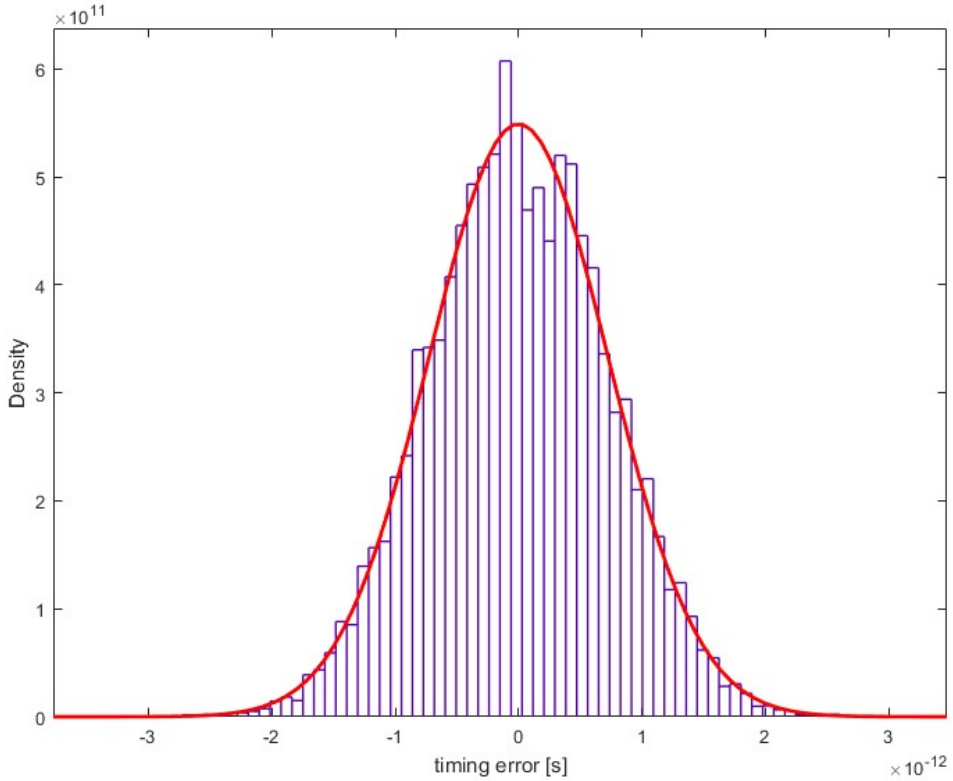
- recorded 1.6M samples
- fitting normal distribution with:

  μ = -2.93117e-21s

  σ = 726.36 fs

- timing error (p2p): 7 ps
- timing error (rms): 726 fs

- results are not outstanding but also not bad
- meet the requirements of ~1 ps



Summary & Outlook

- results of test measurements look promising
- meet the requirements of ~ 1 ps timing error
- operation in FLASH will show wether the accuracy will actually be achieved

- further improvements of the DFMC-DS500 have to be done → second revision
- PLL is not running with full performance (reduction of phase noise and jitter)

ACKNOWLEDGEMENTS

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Thank you for your attention.

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EOBAM System

BAM System's Units & Periphery