10th International Computational Accelerator Physics Conference
San Francisco, Aug .31 – Sept. 4, 2009

Portable High Performance Computing for Microwave Simulation by FDTD/FIT Machines

CONTENTS

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Japan

INTRODUCTION

Background of FDTD/FIT dedicated computers

original ideas
individuals (1980's)
only ideas

original work
J. R. Marek, et.al. (1992)
PC board type, VHDL simulation

advances in FDTD method
(PML, ...)

requirement for HPC of
electromagnetic fields (science & industry)

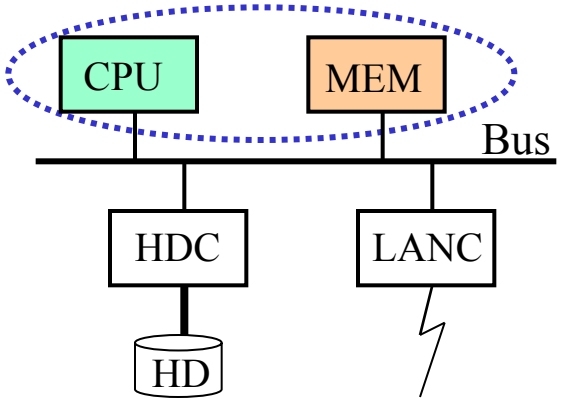
large scale FPGA (more than 1M gates), GPU
LSI design software (VHDL, …..)
low price PCB manufacturing (less than 500 $)

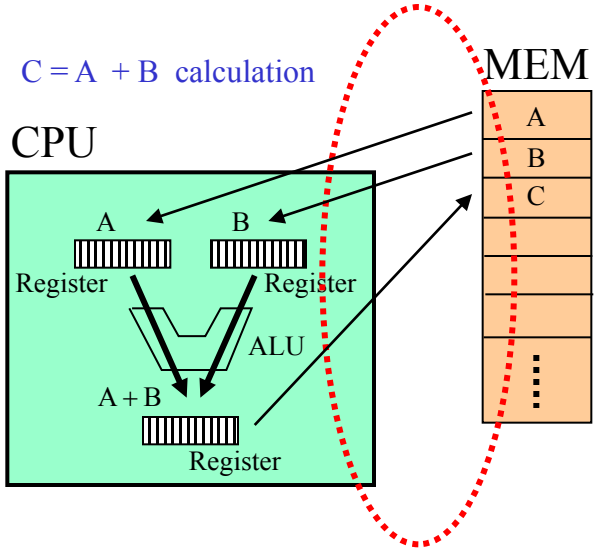
commercial products
R. N. Schneider, et.al. (2004 -)

real hardware
P. Placidi, et.al. (2002 -), PCI board, dedicated computer
R. N. Schneider, et.al. (2002 -), 1D dedicated computer, FPGA, GPU
H. Kawaguchi, et.al. (2002 -), 2D dedicated computer, FPGA, custom PCB
J. P. Durbano, et.al. (2003 -), 3D dedicated computer, FPGA

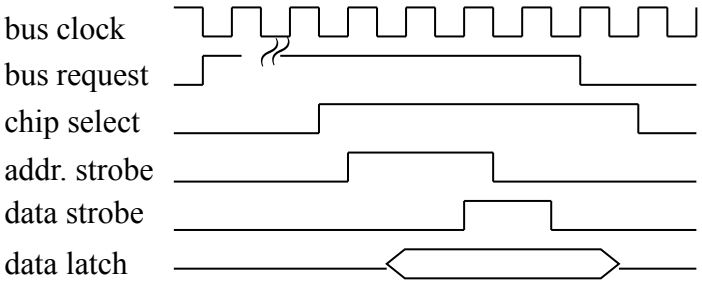
DEDICATED HARDWARE ARCHTECTURE

Neumann bottleneck in mainframe





memory access time chart



Dedicated computer

- no bus architecture
- optimized data flow
- optimized memory allocation

Three parallel properties hidden in FDTD scheme

$$E_{xi,j,k}^{n+1} = E_{xi,j,k}^{n-1} + \frac{\Delta t}{\varepsilon \Delta l}\left[H_{zi,j,k}^{n} - H_{zi,j-1,k}^{n} - H_{yi,j,k}^{n} + H_{yi,j,k-1}^{n}\right]$$

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$$H_{xi,j,k}^{n} = H_{xi,j,k}^{n-1} - \frac{\Delta t}{\mu \Delta l}\left[E_{zi,j+1,k}^{n} - E_{zi,j,k}^{n} - E_{yi,j,k+1}^{n} + E_{yi,j,k}^{n}\right]$$

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all same algebra structure

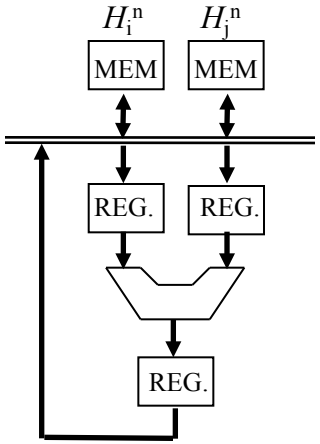
$$E^{n+1} = E^{n-1} + C\left[H_1^n - H_2^n - H_3^n + H_4^n\right]$$

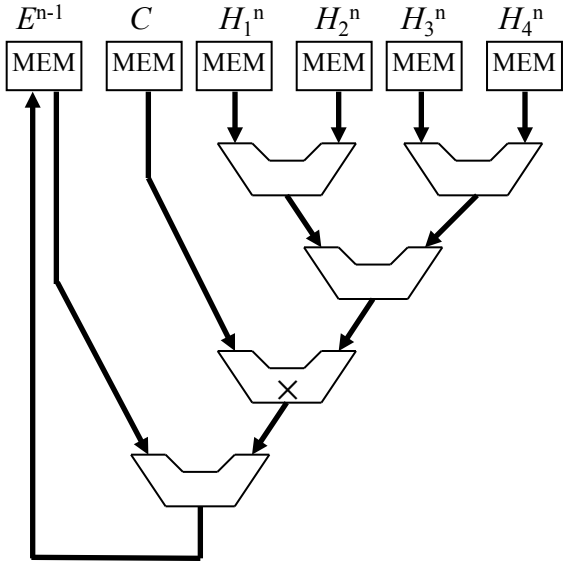
(1) Dataflow property

binary operation

at least 5 clocks

and 7 memory access





dataflow calculation

- memory access
- dataflow circuit

almost single clock

Three parallel properties hidden in FDTD scheme

$$E_{xi,j,k}^{n+1} = E_{xi,j,k}^{n-1} + \frac{\Delta t}{\varepsilon \Delta l}\left[H_{zi,j,k}^{n} - H_{zi,j-1,k}^{n} - H_{yi,j,k}^{n} + H_{yi,j,k-1}^{n}\right]$$

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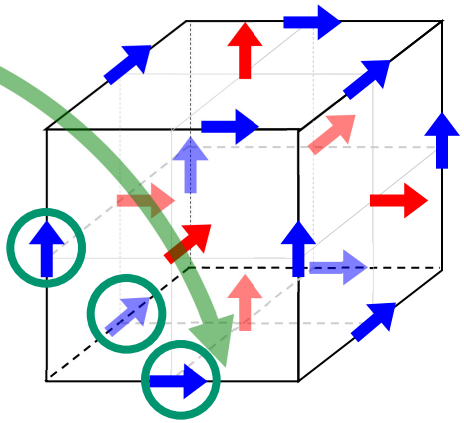
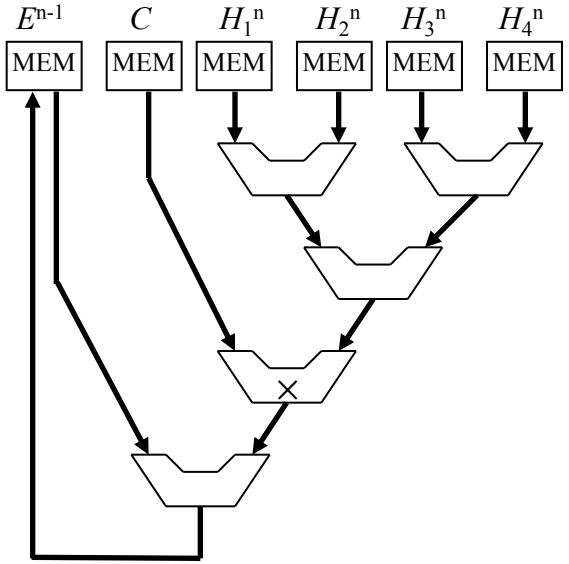
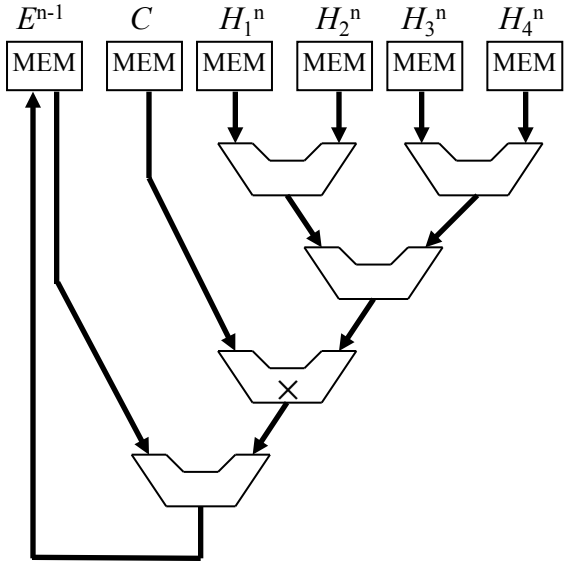
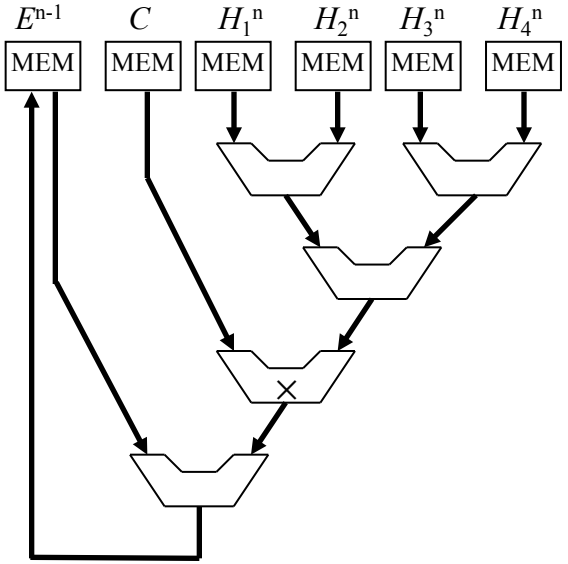
(1) Dataflow property

(2) Parallel cal. of three components









Three parallel properties hidden in FDTD scheme

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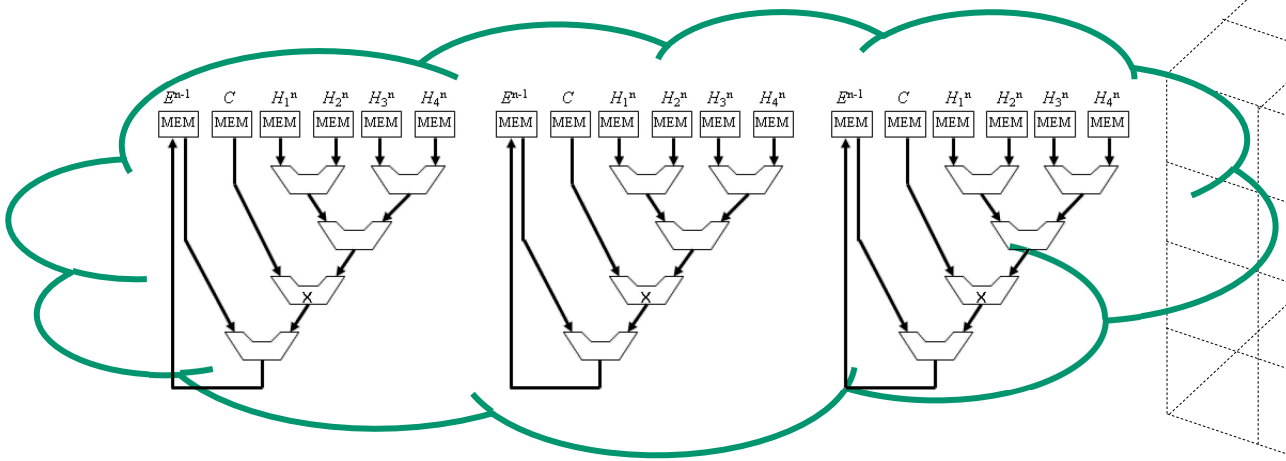
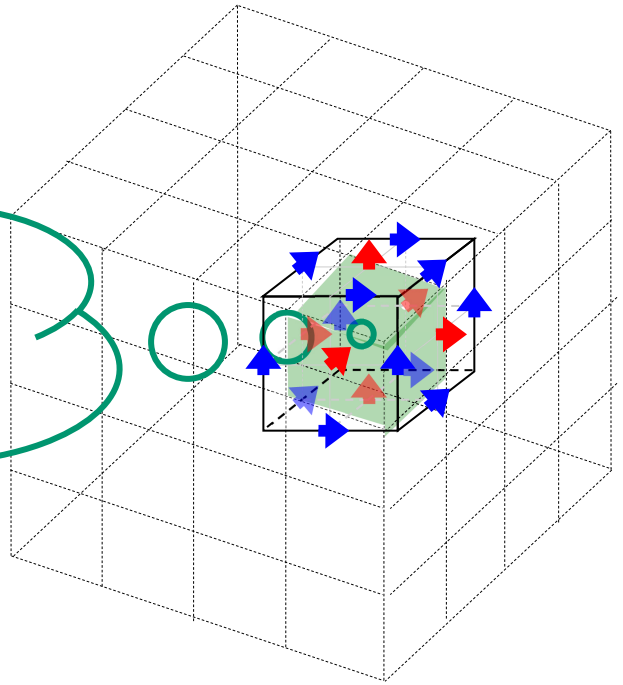
(1) Dataflow property

(2) Parallel cal. of three components

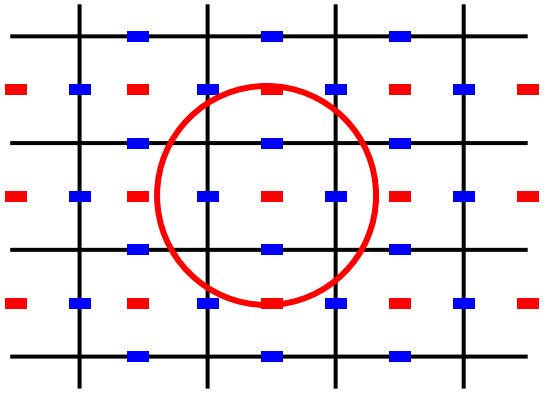
(3) Parallel calculation in grid space





Full dataflow architecture FDTD / FIT machine (2D)

FDTD/FIT grid space



(1) Dataflow property
(2) Parallel cal. of three components
(3) Parallel calculation in grid space

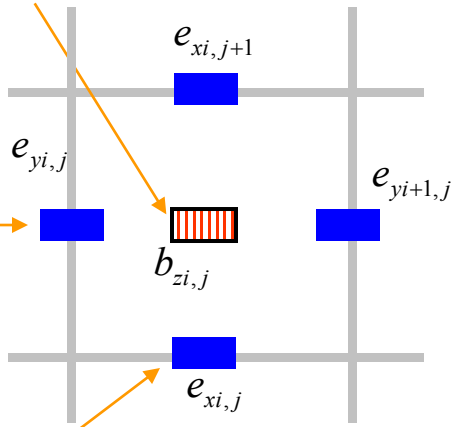
allocation of register

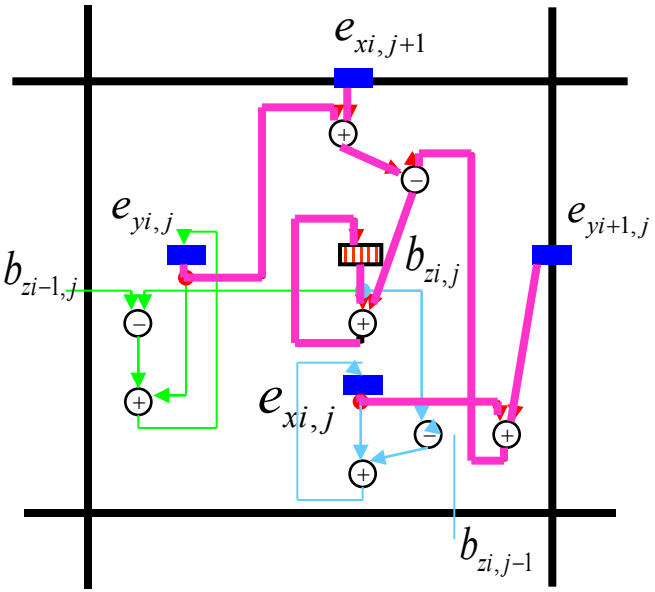
connection according to FDTD scheme

$$b_{zi,j}^{n+1/2} = b_{zi,j}^{n-1/2} - \frac{1}{2}(e_{xi,j}^{n} + e_{yi+1,j}^{n} - e_{xi,j+1}^{n} - e_{yi,j}^{n})$$

$$e_{yi,j}^{n} = e_{y\ j}^{n\ \cdot 1} - \frac{1}{2}(b_{zi,j}^{n-1/2} - b_{zi-1,j}^{n-1/2})$$

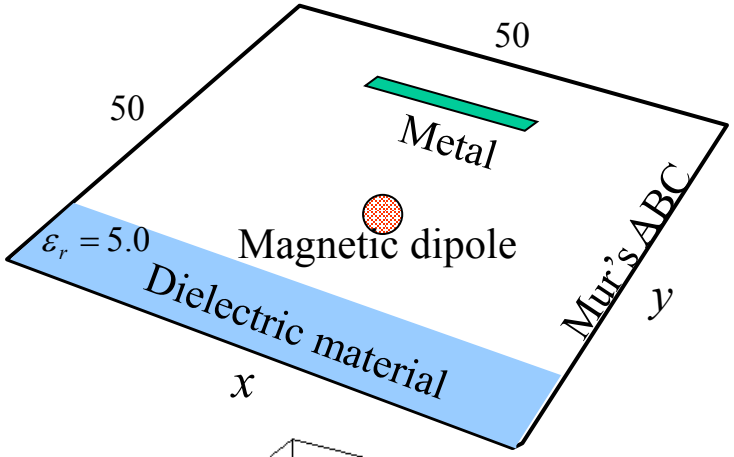
$$e_{xi,j}^{n} = e_{xi,j}^{n-1} + \frac{1}{2}(b_{zi,j}^{n-1/2} - b_{zi,j-1}^{n-1/2})$$

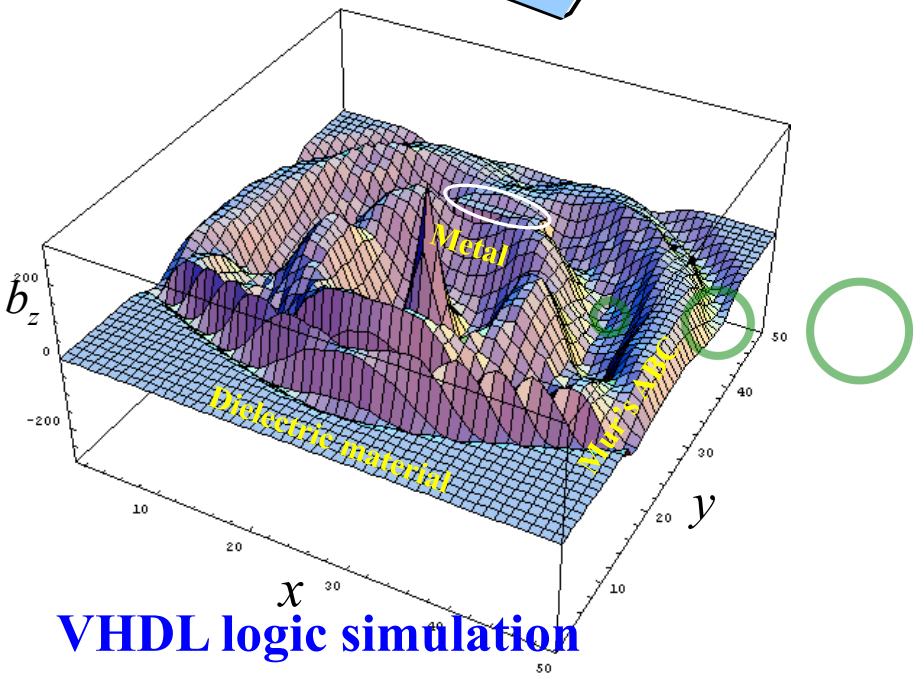




Full dataflow architecture FDTD / FIT machine (2D)

Numerical model



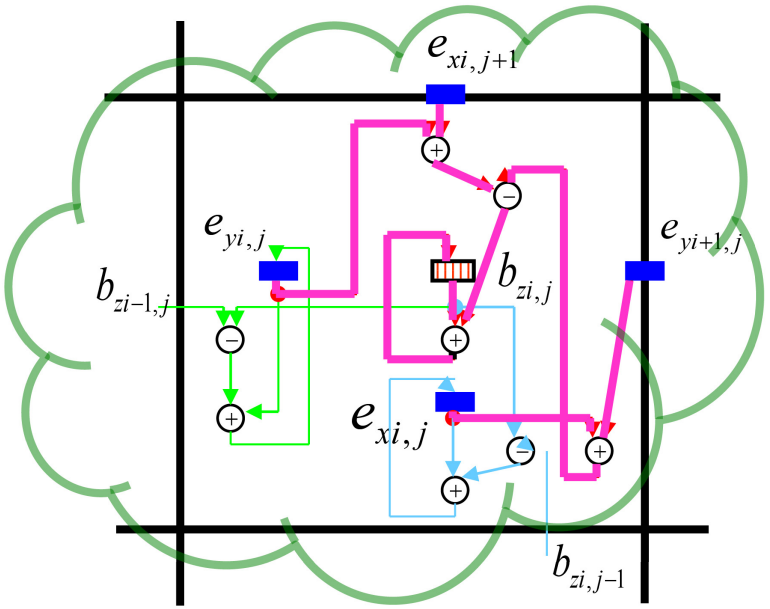


VHDL logic simulation

(1) Dataflow property
(2) Parallel cal. of three components
(3) Parallel calculation in grid space

- very simple operation
- very high speed calculation

- huge hardware size
- fixed grid size (poor flexibility)

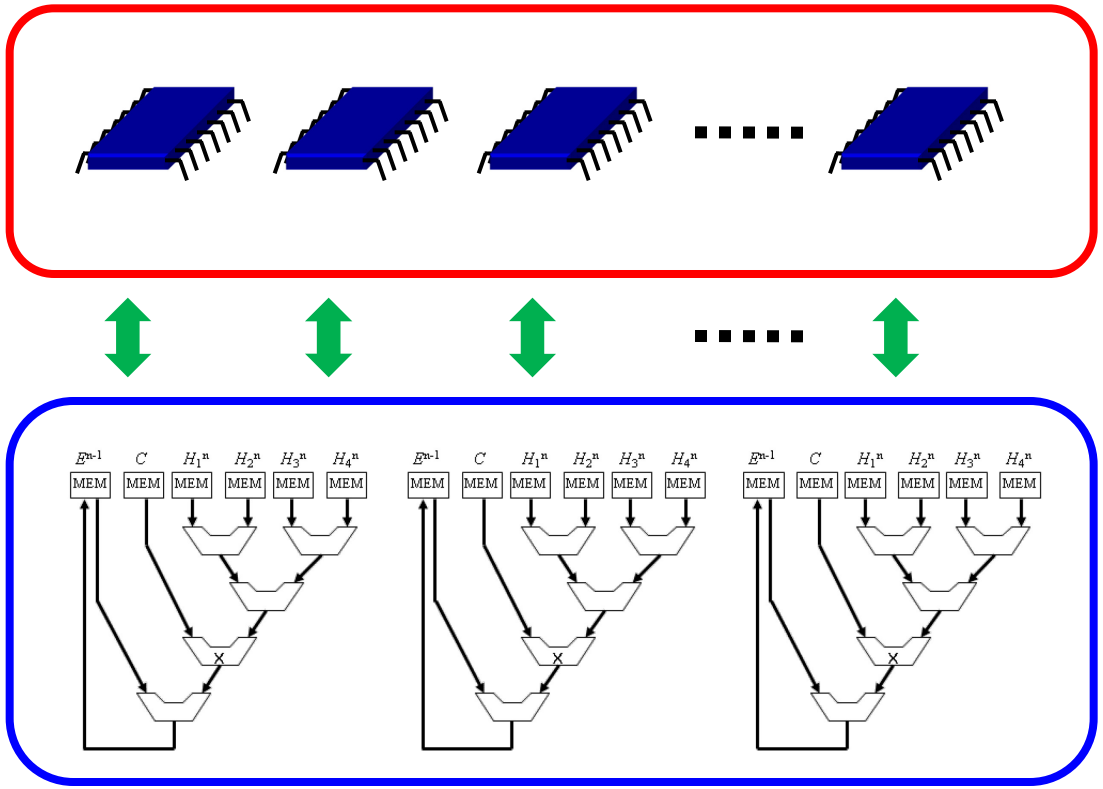


Memory architecture FDTD / FIT machine

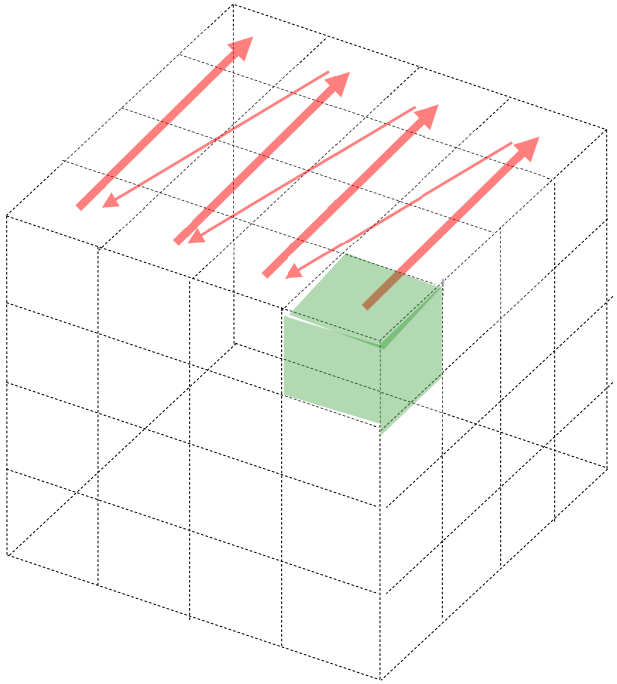
(1) Dataflow property
(2) Parallel cal. of three components
(3) Parallel calculation in grid space

- very simple operation
- very **high speed calculation**
- **reasonable hardware size**
- **rich flexibility**

MEMORY MODULE



CALCULATION MODULE



Memory architecture FDTD / FIT machine

$$E_{xi,j,k}^{n+1} = E_{xi,j,k}^{n-1} + \frac{\Delta t}{\varepsilon \Delta l}\left[H_{zi,j,k}^{n} - H_{zi,j-1,k}^{n} - H_{yi,j,k}^{n} + H_{yi,j,k-1}^{n}\right]$$

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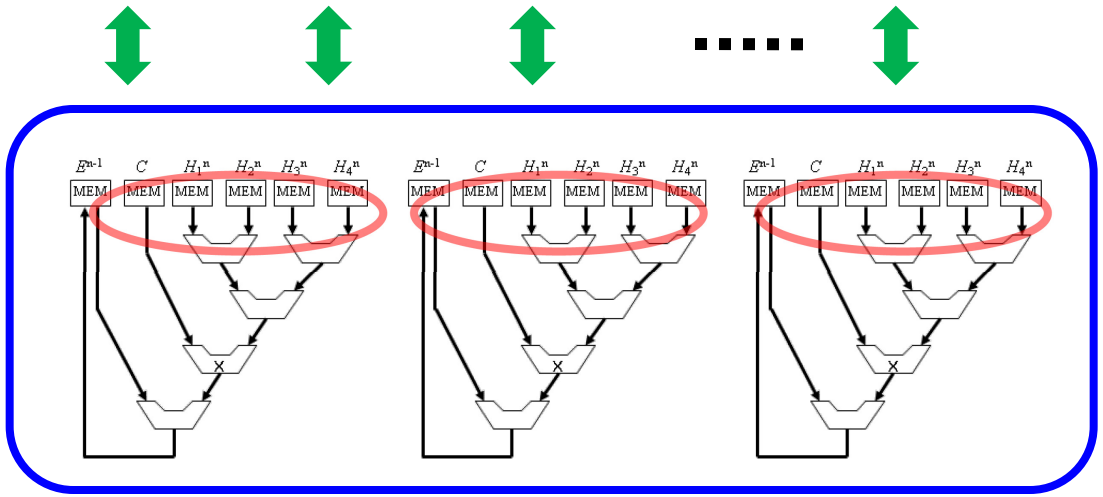
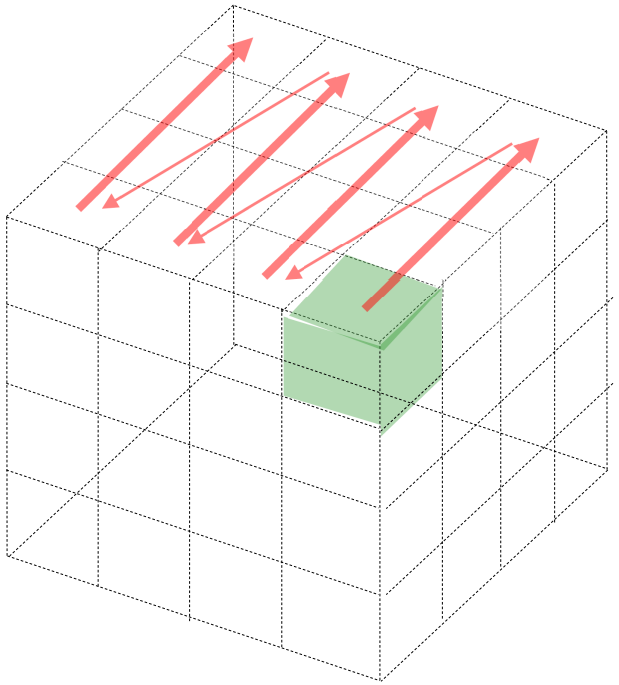
parallel access to 12 different field values are required for parallel computation of three field components





CALCULATION MODULE

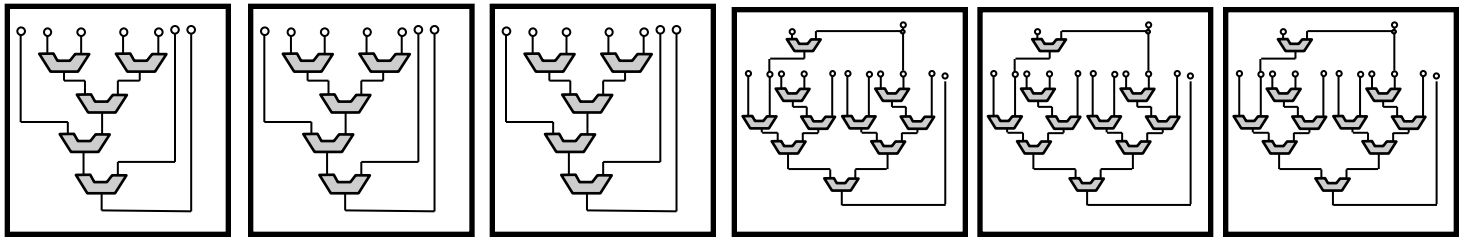
Parallel access memory architecture

MEMORY MODULE

Boundary Condition		Grid Information		Input Signals	
e_x	e_y	e_z	b_x	b_y	b_z
Memory1 (i,j,k)	Memory1 (i,j,k)	Memory1 (i,j,k)	Memory1 (i,j,k)	Memory1 (i,j,k)	Memory1 (i,j,k)
Memory2 (i,j+1,k)	Memory2 (i+1,j,k)	Memory2 (i+1,j,k)	Memory2 (i,j-1,k)	Memory2 (i-1,j,k)	Memory2 (i-1,j,k)
Memory3 (i,j,k+1)	Memory3 (i,j,k+1)	Memory3 (i,j +1,k)	Memory3 (i,j,k-1)	Memory3 (i,j,k-1)	Memory3 (i,j-1,k)
Memory4 PML e_{xy}	Memory4 PML e_{yz}	Memory4 PML e_{zx}	Memory4 PML b_{xy}	Memory4 PML b_{yz}	Memory4 PML b_{zx}

Selector Circuit

Normal Grid **PML**



CALCULATION MODULE

Boundary conditions (dielectric & magnetic materials)

$$
\begin{aligned}
E_{xi,j,k}^{n+1} &= E_{xi,j,k}^{n-1} + \frac{\Delta t}{\varepsilon \Delta l}\left[H_{zi,j,k}^{n} - H_{zi,j-1,k}^{n} - H_{yi,j,k}^{n} + H_{yi,j,k-1}^{n}\right] \\
E_{yi,j,k}^{n+1} &= E_{yi,j,k}^{n-1} + \frac{\Delta t}{\varepsilon \Delta l}\left[H_{xi,j,k}^{n} - H_{xi,j,k-1}^{n} - H_{zi,j,k}^{n} + H_{zi-1,j,k}^{n}\right] \\
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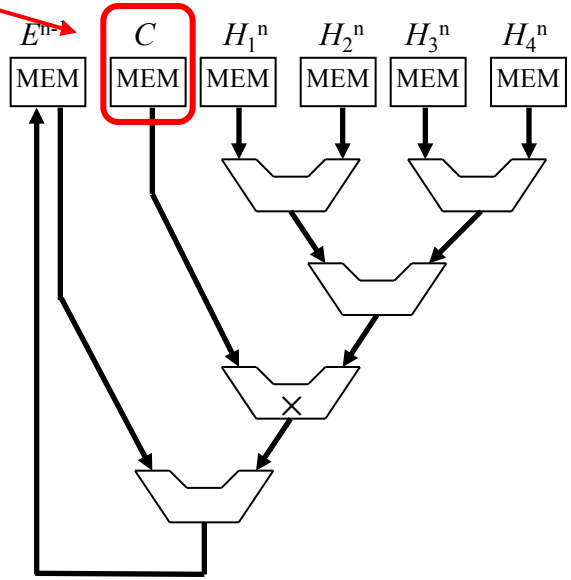
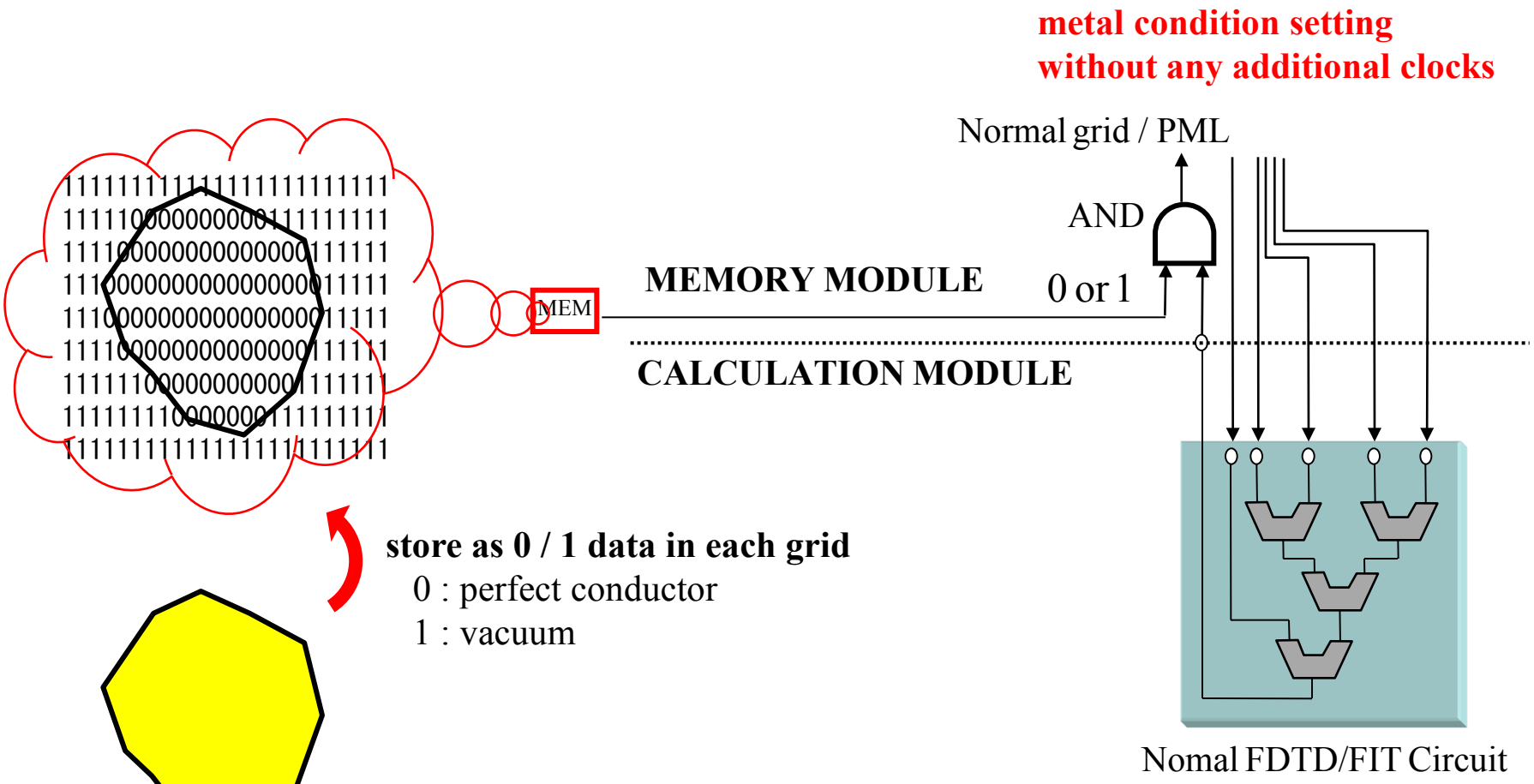
\end{aligned}
$$

$$
E^{n+1} = E^{n-1} + C\left[H_1^n - H_2^n - H_3^n + H_4^n\right]
$$

material constants are stored for every grids



Boundary conditions (perfect conductor / metal)



Boundary conditions (PML ABC)

$$\varepsilon_0 \frac{\partial E_{xy}}{\partial t} + \sigma_y E_{xy} = \frac{\partial (H_{zx} + H_{zy})}{\partial y}$$

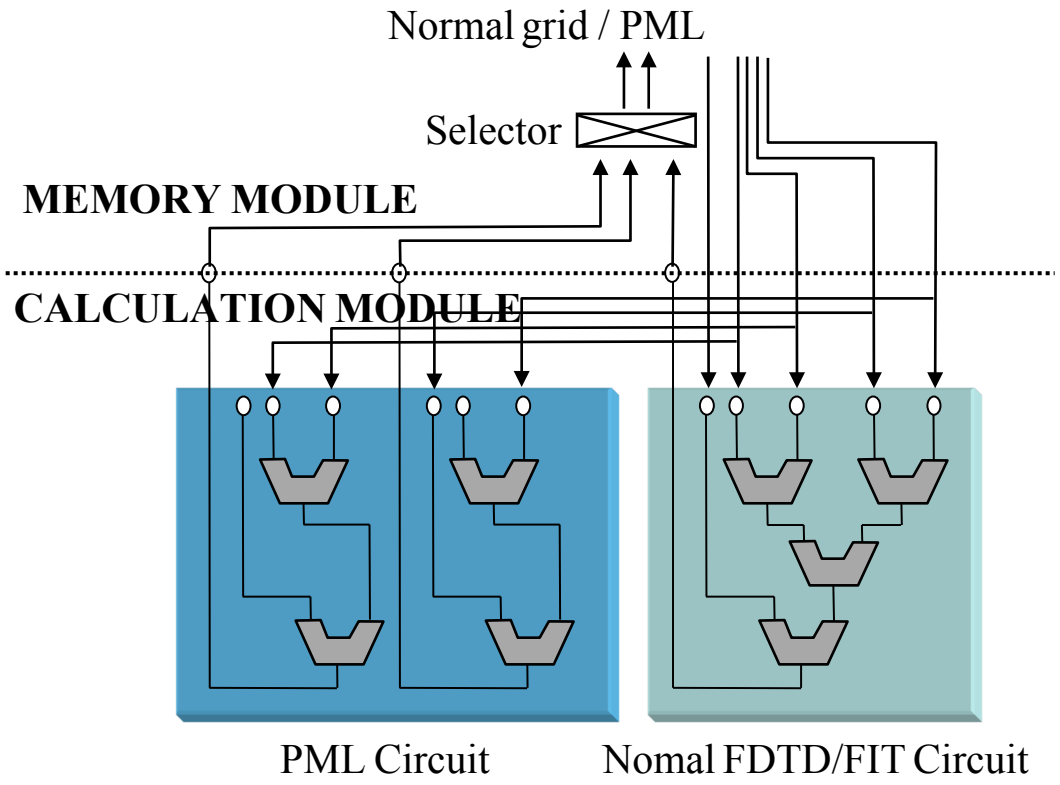
$$\varepsilon_0 \frac{\partial E_{xz}}{\partial t} + \sigma_z E_{xz} = -\frac{\partial (H_{yz} + H_{yx})}{\partial z}$$

$$\varepsilon_0 \frac{\partial E_{yz}}{\partial t} + \sigma_z E_{yz} = \frac{\partial (H_{xy} + H_{xz})}{\partial z}$$

$$\varepsilon_0 \frac{\partial E_{yx}}{\partial t} + \sigma_x E_{yx} = -\frac{\partial (H_{zx} + H_{zy})}{\partial x}$$

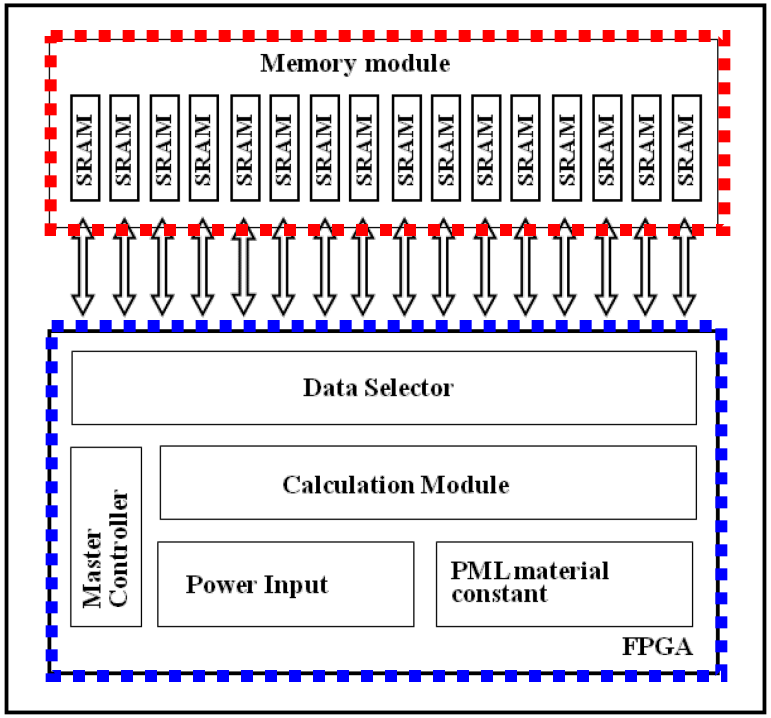
$$\varepsilon_0 \frac{\partial E_{zx}}{\partial t} + \sigma_x E_{zx} = \frac{\partial (H_{yz} + H_{yx})}{\partial x}$$

$$\varepsilon_0 \frac{\partial E_{zy}}{\partial t} + \sigma_y E_{zy} = -\frac{\partial (H_{xy} + H_{xz})}{\partial y}$$

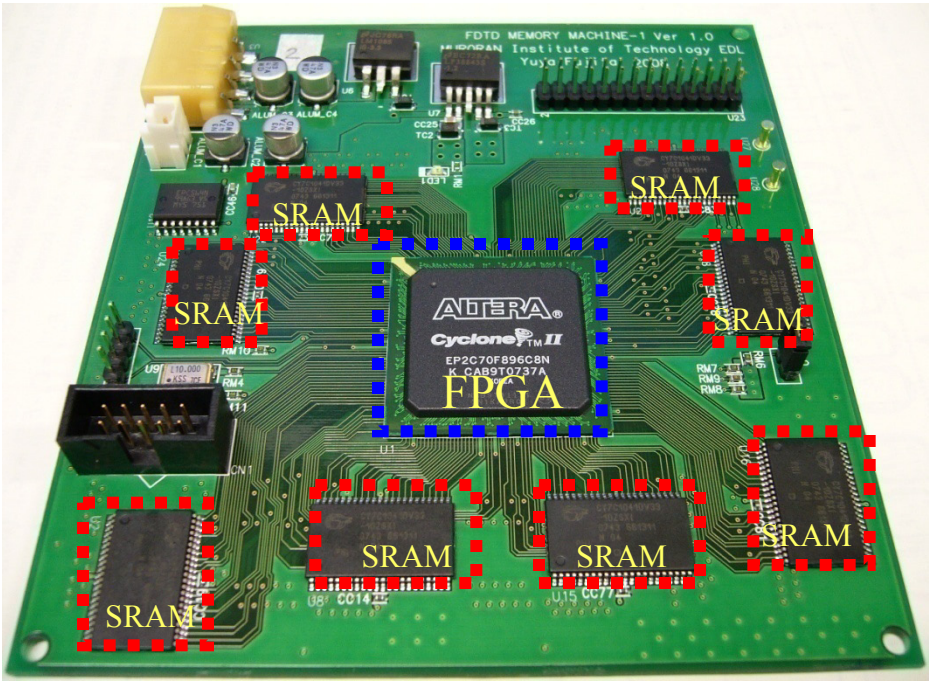


IMPLEMENTATION IN HARDWARE

Full custom PCB of FDTD/FIT memory architecture machine



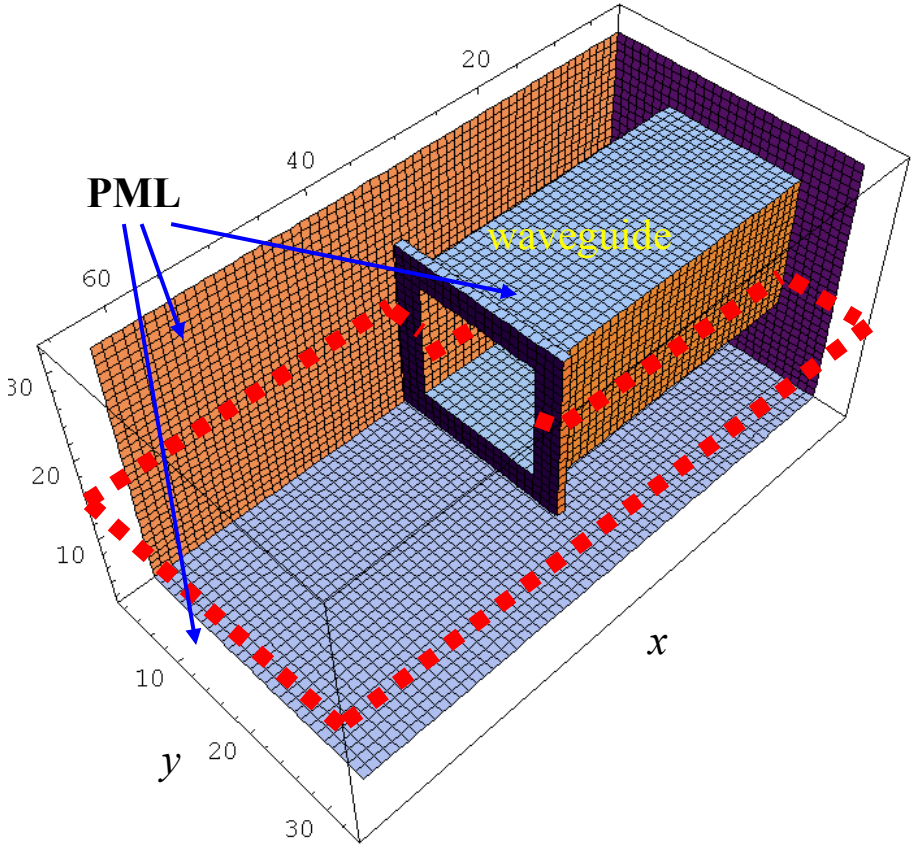
hardware configuration



top view

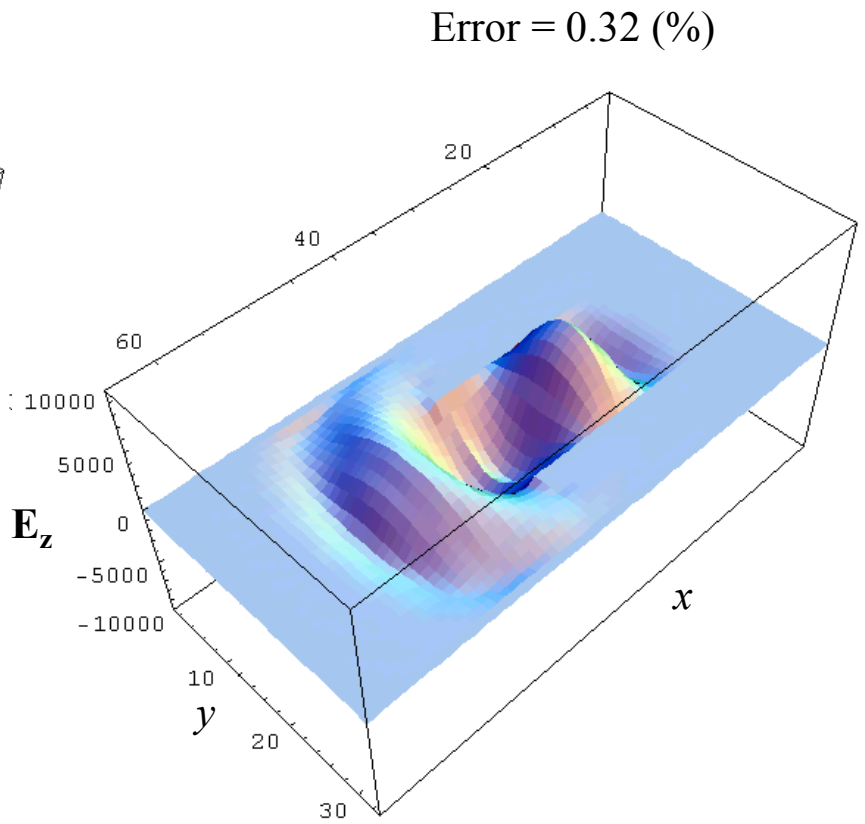
MACHINE OPERATION

Numerical model



Numerical model

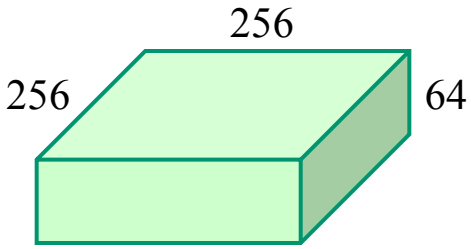
Simulation result



E_z Component of Electric field at z = 15 plane

SUMMARY

Summary



- Design of full 3D FDTD/FIT dedicated computer
- Development of custom printed circuit board

Performance

2.5 times higher than PC with Core2 Duo (3.16GHz, 4GB)
in 51MHz FPGA clock operation

Cost

about 1,600 $ / PCB (parts : 300, board : 700, equip : 600)

Future Problems

- Parallel calculation by interlocking operation of FDTD/FIT machines
- PC control interface (including user interface)
- FPGA circuit optimization (for higher frequency operation --> 166 MHz)
- Introduction of advanced scheme such as PBA FIT, ...
- DDR like memory architecture, ...

SDRAM frequency